

POS-PIQ57BQ

Revision: R1.01 (2010/04/20)

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64	+1P05V_PCH / +1P05V_ME
65	+5V_DUAL / +3P3V_ME
66	+SM_VTT / +1P8V_SFR

## Schematics Change History

[illegible]

**CAD Note:**

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

Property: BOM

I = Installed Part.

NI = Not Installed Part.

PROTO = PROTO Phase Only.

VP = Virtual Part.

**PEGATRON DT-MB RESTRICTED SECRET**

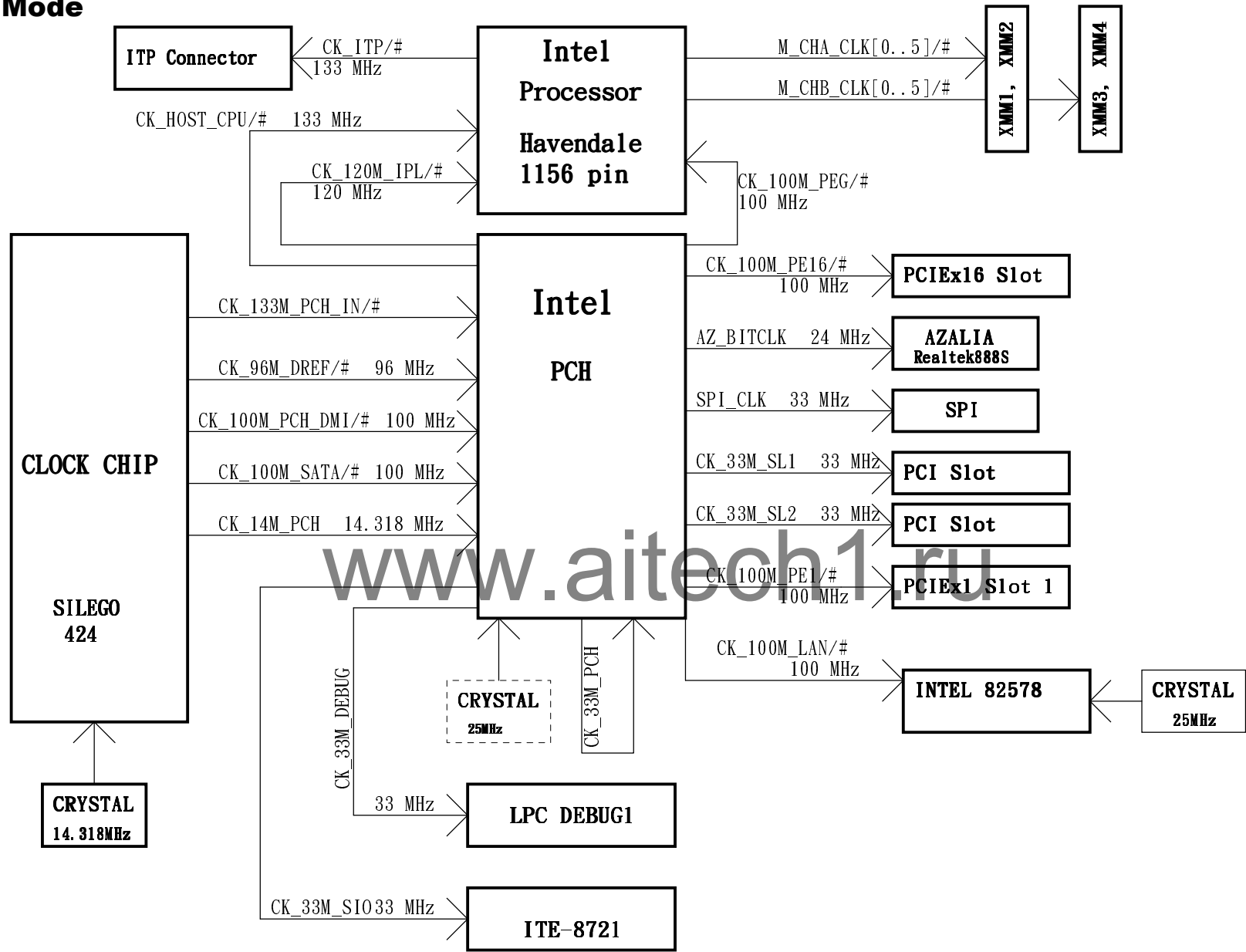
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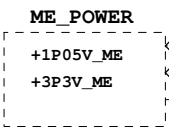
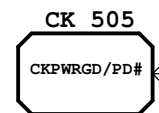
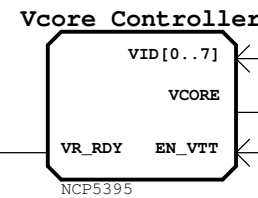
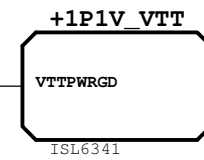
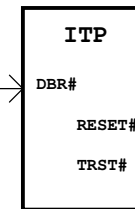
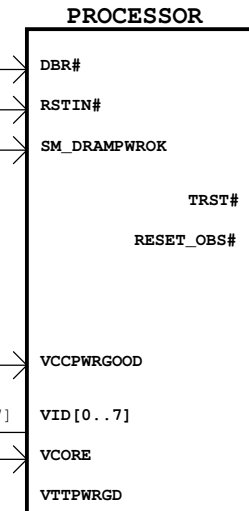
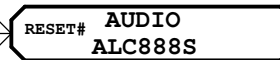
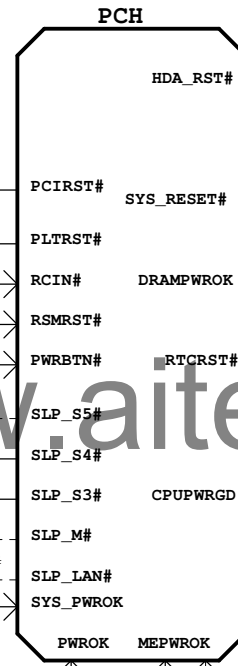
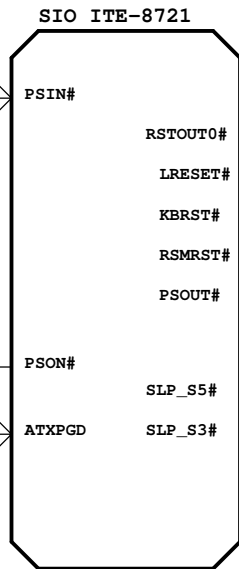
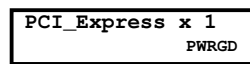
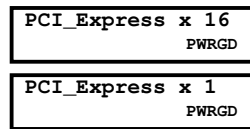
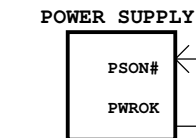
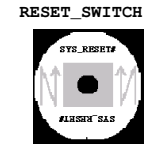
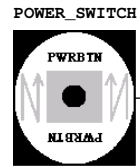
Pegatron Corp. **Engineer:** Vic Chen

Size	Project Name	Rev
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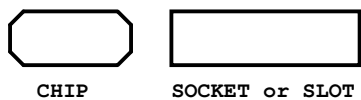
PCH Buffer Mode



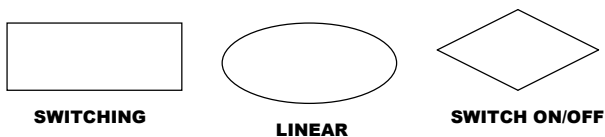
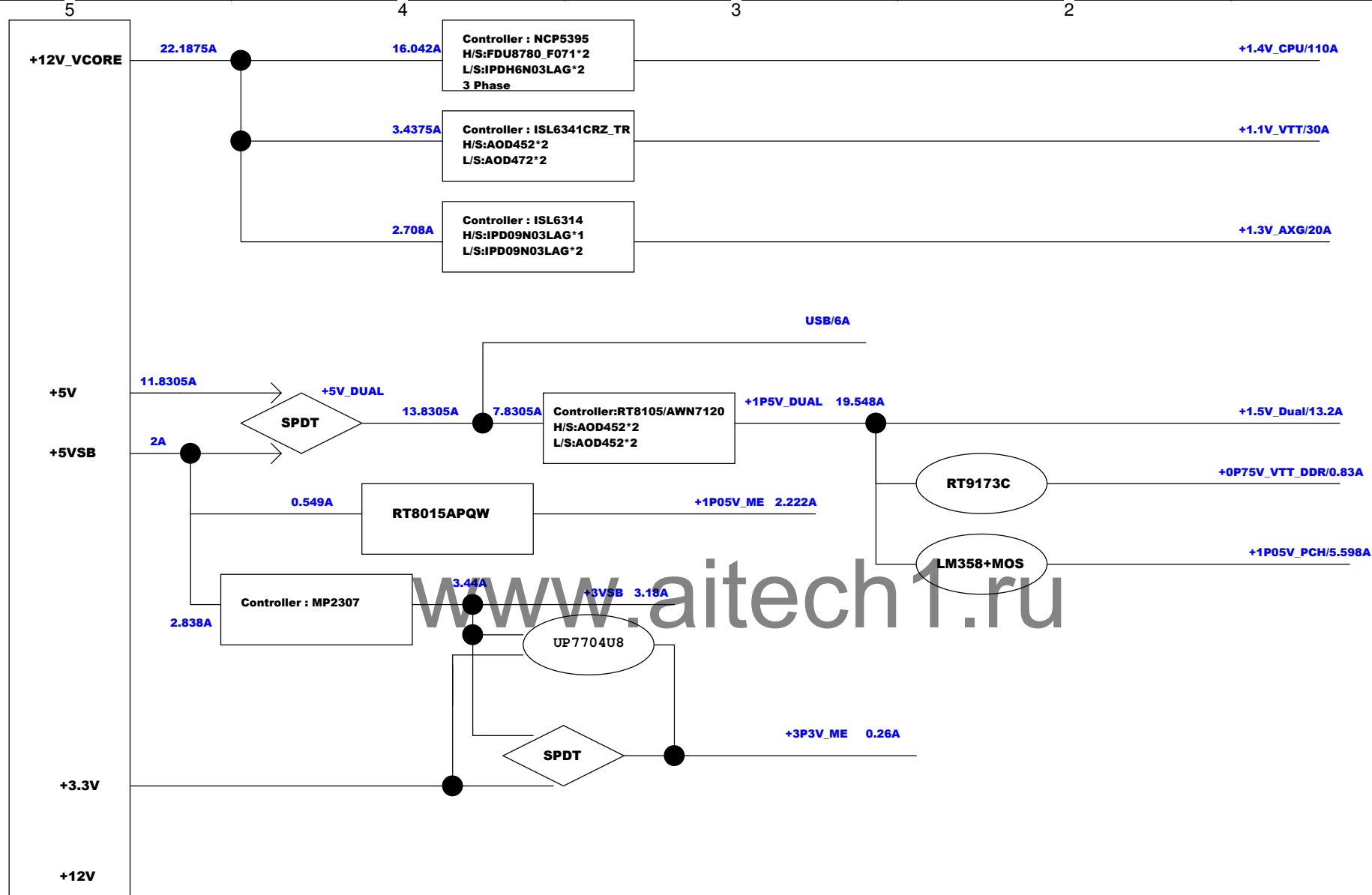


If support AMT, SLP\_M#  
will come with SLP\_S5

If not support AMT, SLP\_M#  
will come with SLP\_S3







<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER FLOW</b>	
PEGATRON CORPORATION		Engineer: <b>Michael Lee</b>	
Size A3	Project Name <b>IPMIP-DP</b>		Rev 1.01
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Lynnfield/Clarkdale	
VCORE	-> 90A - 95(TBD)W
+1.1V_VTT	-> 30A(TBD) - 33W
+1.5V	Vddq -> 6A - 9W
+1.8V	Vccpll -> 1.35A - 2.43W

Intel Ibox Peak	
V_CPU_IO	-> <1mA - 1.1mW
+5V	V5REF -> <1mA - 5mW
+5V	V5REF_Sus -> <1mA - 5mW
+3.3V	Vcc3_3 -> 0.357A - 1.178W VccDAC -> 0.069A - 0.228W
+1.1V	VccDMI -> 0.065A - 0.07W
+1.05V	VccADPLL -> 0.075A - 0.079W VccADPLLb-> 0.075A - 0.079W VccCORE -> 1.629A - 1.71W VccIO -> 3.251A - 3.414W VccLAN -> 0.372A - 0.39W VccME -> 2.222A - 2.333W
+1.8V	VccqNAND -> 0.156A - 0.281W VccVRM -> 0.196A - 0.353W VccTX_LVDS -> 0.059A - 0.106W
+3P3V	VccALVDS -> <1mA - 3.3mW
+3P3VSB	VccRTC -> 2mA - 6.6mW VccSus3_3 -> 0.168A - 0.554W VccSusHDA -> 0.006A - 0.02W VccME3_3-> 0.086A - 0.284W

CLOCK- CK505	
+3P3V	-> 250mA - 0.825W
+VDD_IO (0.8V)	-> 80mA - 64mW

DDR3 DIMM (4) & Termination	
+1.5V_DAUL	VDD (S0, S1) -> 7.2 A - 10.8W VDD (S3) -> 712mA - 1.07W
SM_VTT(0.75V)	SM VTT (S0, S1) -> 0.83A - 0.623W

PCI Express x 1	
+12V	-> 0.5A - 6W
+3P3V	-> 3.0A - 9.9W
+3P3V_PCI	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

PCI Express x 16	
+12V	-> 5.5A - 66W
+3P3V	-> 3.0A - 9.9W
+3P3V_PCI	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

PCI SLOTS	
+12V	-> 0.5A - 6W
-12V	-> 0.1A - 1.2W
+5V	-> 5.0A - 25W
+3P3V	-> 7.6A - 25.08W
+3P3V_PCI	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

INTEL 82578	
+3P3V_CL	-> 15.5mA (TBD) - 51.15mW
+1P8VSB_LAN	-> 300mA - 540mW
VCC_LAN (1.05V)	-> 300mA -315mW

S10 ITE-8721	
+5V	-> 1mA - 5mW
+3.3VSB	-> 2.4uA - 7.92uW
+3.3V	-> 2mA - 6.6mW

ALC888S Azalia Codec	
+5VSB	-> 0.6A - 3W
+3P3V	-> 0.4A - 1.32W

USB 12 PORTS	
+5V_DUAL	(S0, S1) -> 8.4A - 42W (S3) -> 0.336A - 1.68W

1394A	
+3P3V	-> mA - W

HDMI	
+3P3V	-> mA - mW
+2P5V_DVI	-> mA - mW

SATA 6 PORTS	
+5V	-> 0.975A - 4.875W
+12V	-> 0.9A - 10.8W

FAN	
+12V	-> 0.6A - 7.2W

PS2 KB/MS	
+5V_DUAL	(S0, S1) -> 0.345A - 1.73W (S3) -> 2mA - 10mW

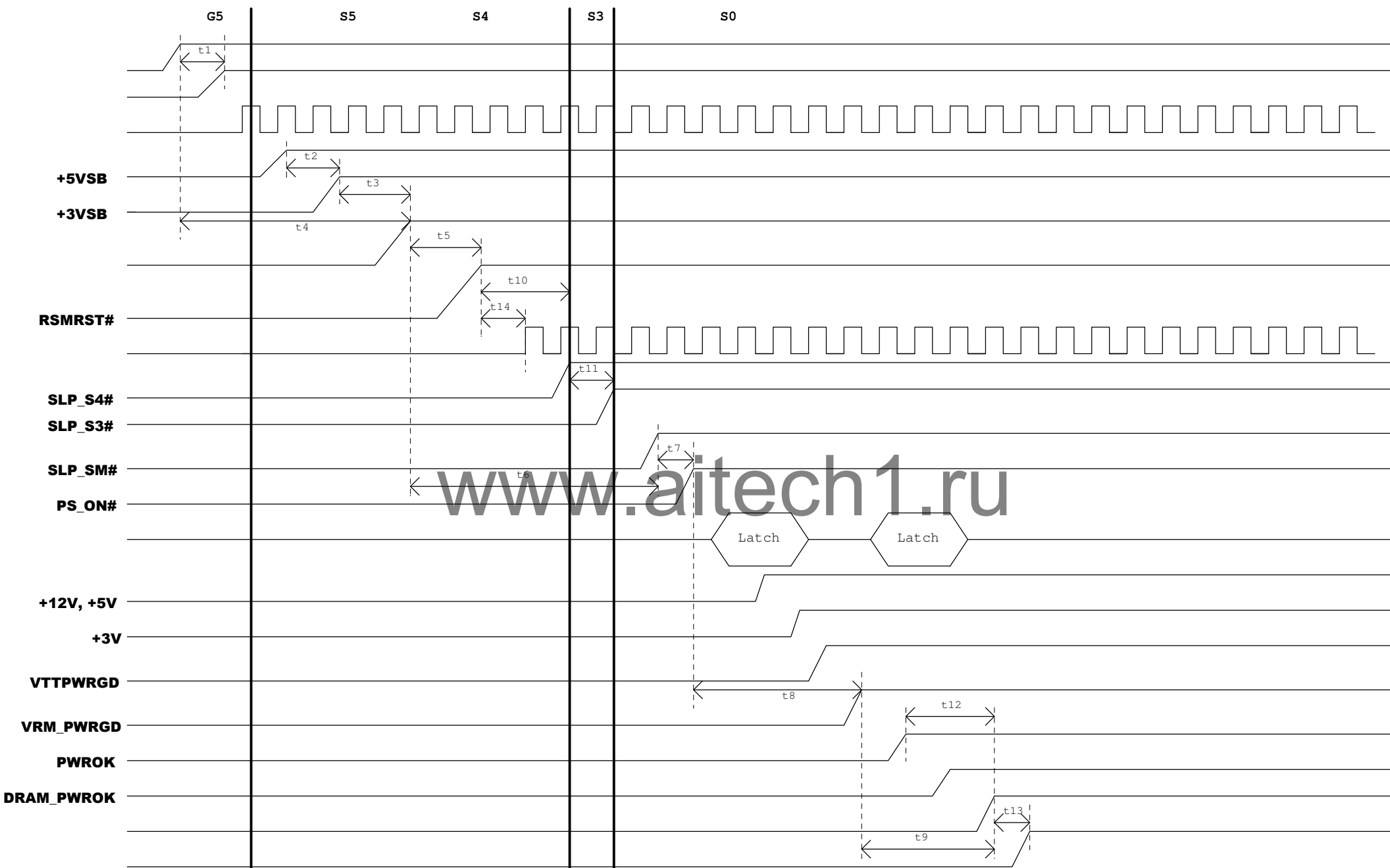
SPI	
+3V	-> 30mA - 99mW

HDD	
+12V	-> 0.75A - 9.0W
+5V	-> 0.75A - 3.75W

CD ROM	
+12V	-> 0.75A - 9.0W
+5V	-> 0.75A - 3.75W

PEGATRON DT-MB RESTRICTED SECRET

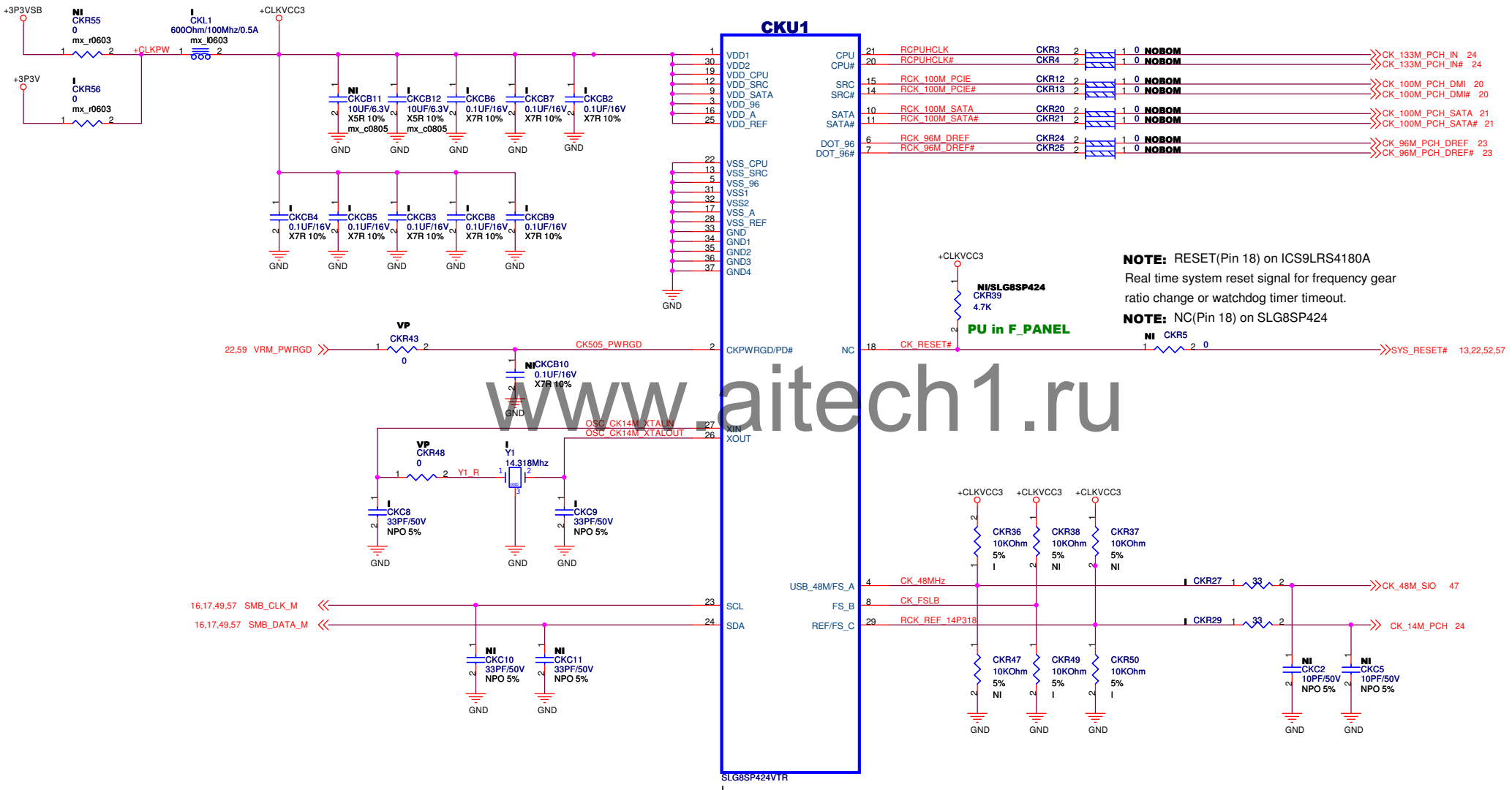
PEGATRON		Title : POWER DISTRIBUTION	
Pegatron Corp.		Engineer:	Vic_Chen
Size A3	Project Name	IPMIP-DP	Rev 1.01
Date:	Tuesday, March 23, 2010	Sheet	6 of 68



The data is not final

- t1>18ms
- t2>0ms
- t4>0ms
- t5>10ms
- t6>0ms
- t7>0ms
- t9>99ms
- t10<110ms
- t11>1RTCCLK
- t12>5ms
- t13:35~74RTCCLK
- t14<110ms

ICS9LRS4180AKLFT: 0610-0038000  
SLG8SP424VTR: 0610-007D000



**NOTE:**

FSLC	FSLB	FSLA	CPU FREQ
0	0	1	133MHz
1	0	1	100MHz

PEGATRON DT-MB RESTRICTED SECRET

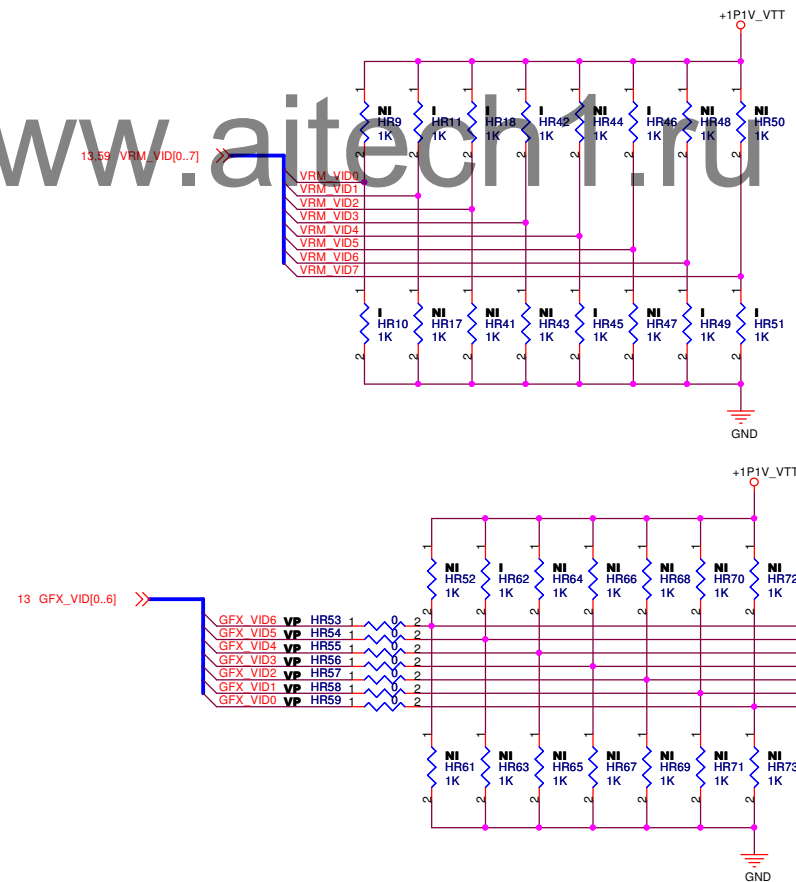
**PEGATRON** Title : ICS 4180/SLG 424

Pegatron Corp. Engineer: Vic\_Chen

Size A3 Project Name IPMIP-DP Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 8 of 68

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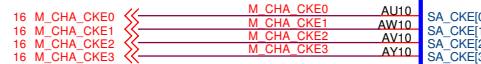
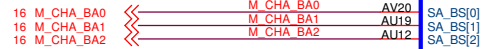
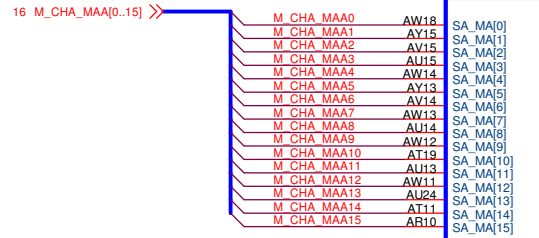


POWER ON CONFIGURATION (POC) TABLE

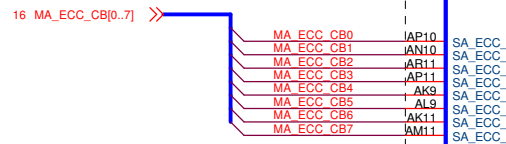
	FUNCTION	DEFAULT
VID0	MSI0	0
VID1	MSI1	1
VID2	MSI2	1
VID3	IMON CONFIG0	1
VID4	IMON CONFIG1	0
VID5	IMON CONFIG3	1
VID6	RESERVED	
VID7	VRD SELECT	LOW
PSI#	RESERVED	LOW

PEGATRON DT-MB RESTRICTED SECRET

<b>PEGATRON</b>		Title : VID RES	
Pegatron Corp.		Engineer: Vic_Chen	
Size A3	Project Name IPMIP-DP	Rev 1.01	
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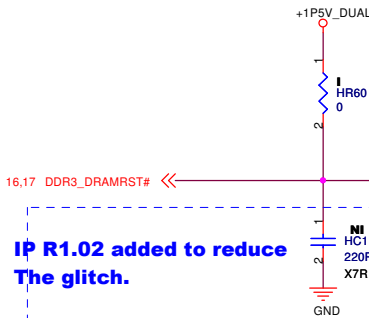
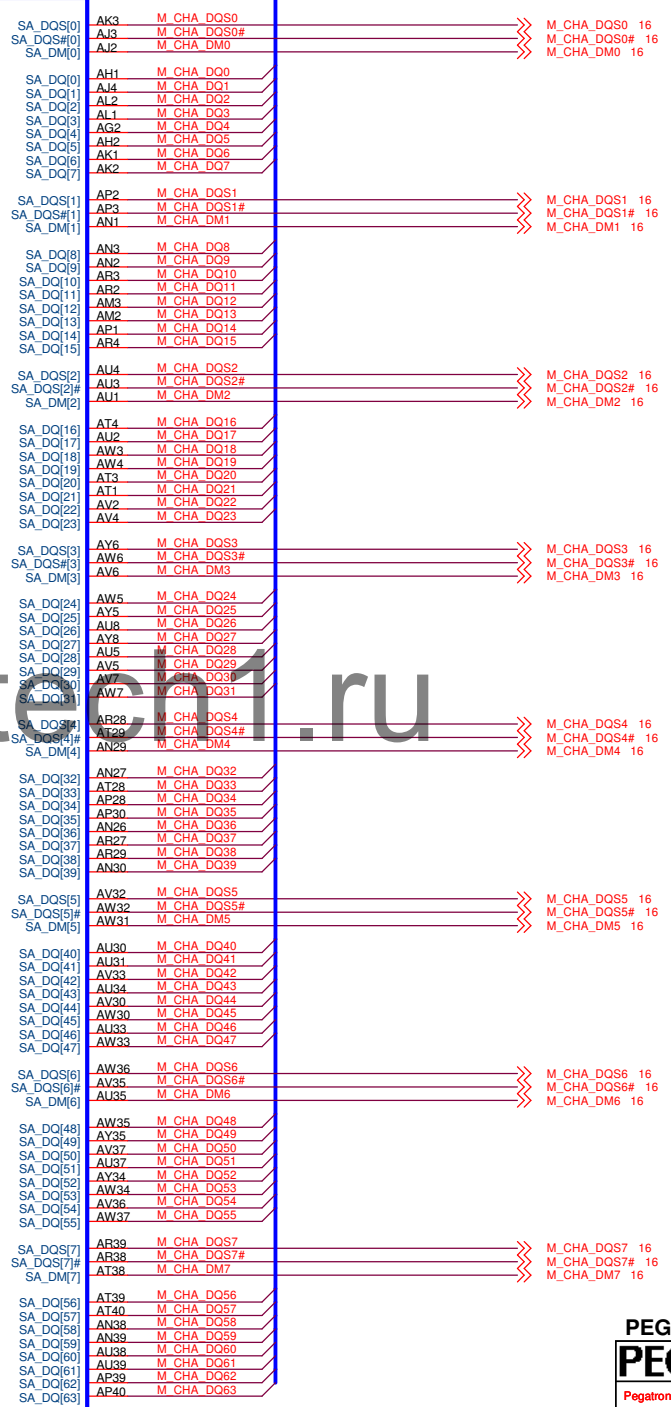
**NOTE:**  
For ECC DIMM



DDR\_A

SOCKET\_1156P

Rev 1.2



IP R1.02 added to reduce  
The glitch.

PEGATRON DT-MB RESTRICTED SECRET

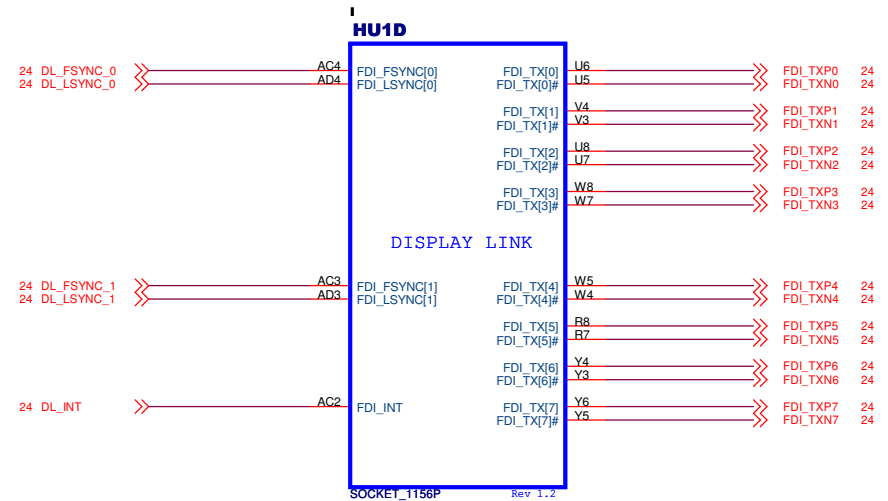
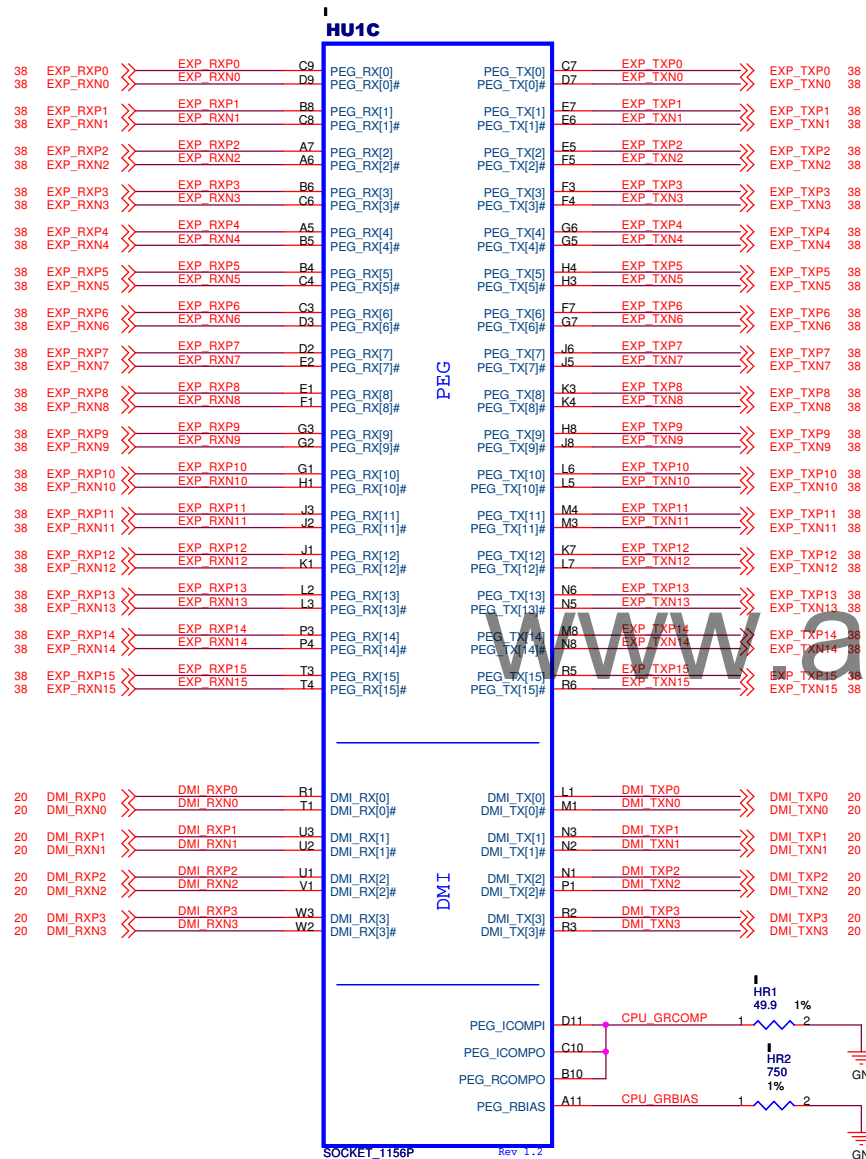
PEGATRON Title : CPU 1160 + MEMORY - 1

Pegatron Corp. Engineer: Vic\_Chen

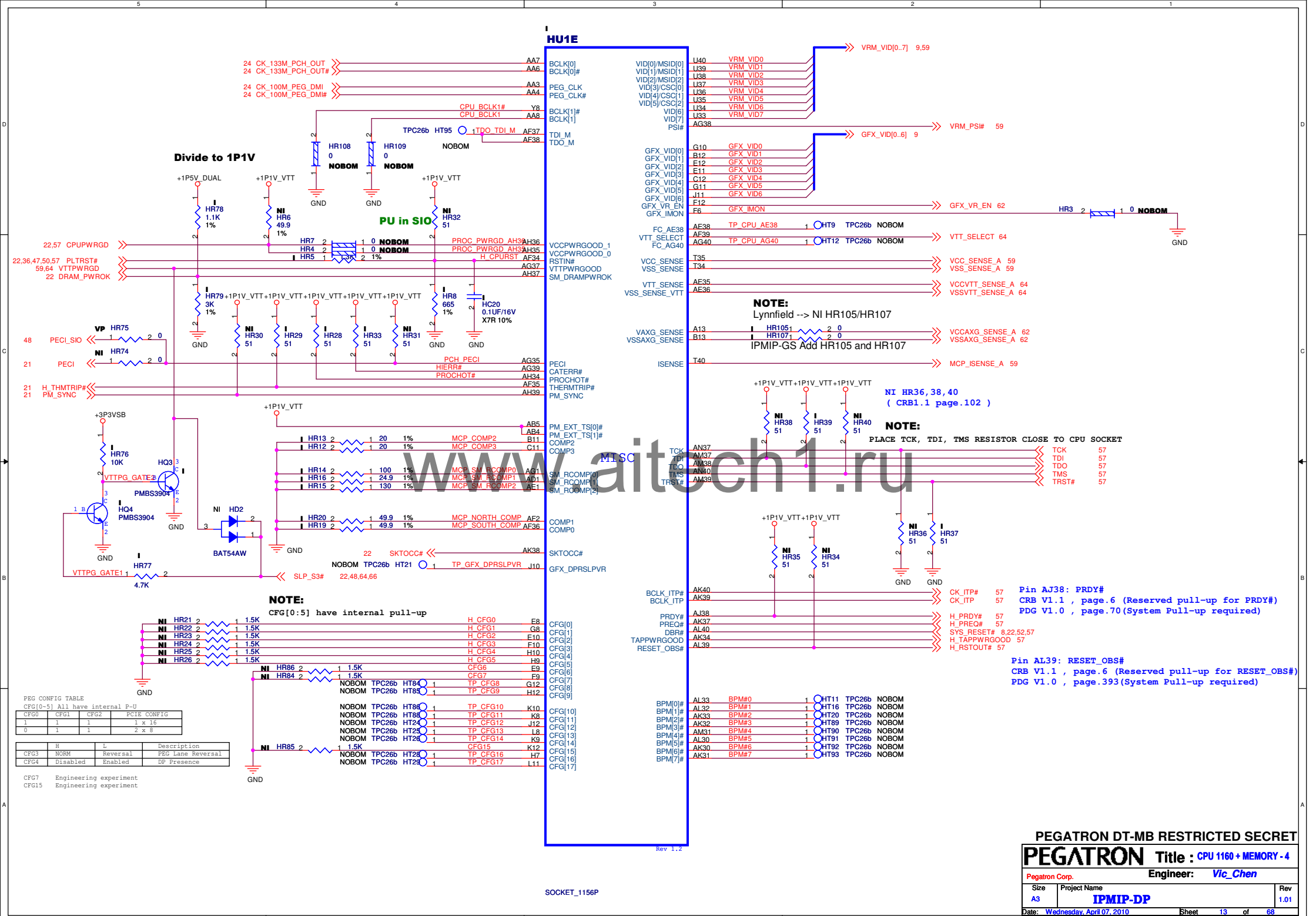
Size A3 Project Name IPMP-IP

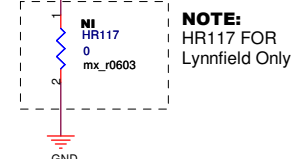
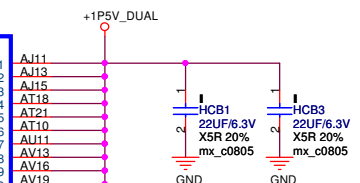
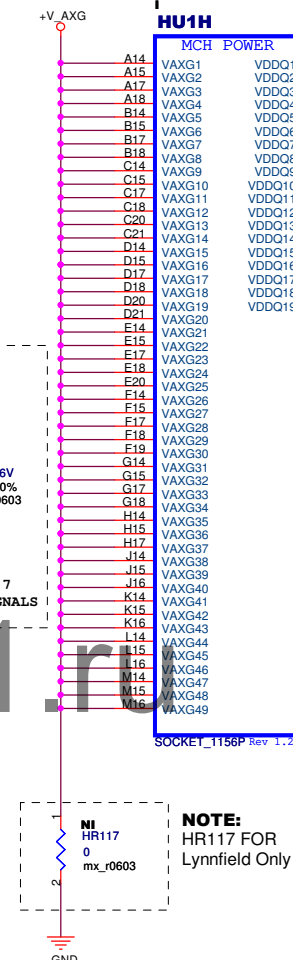
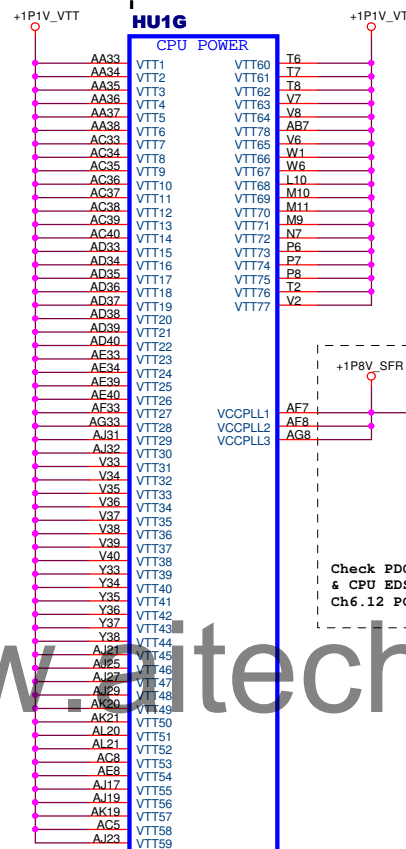
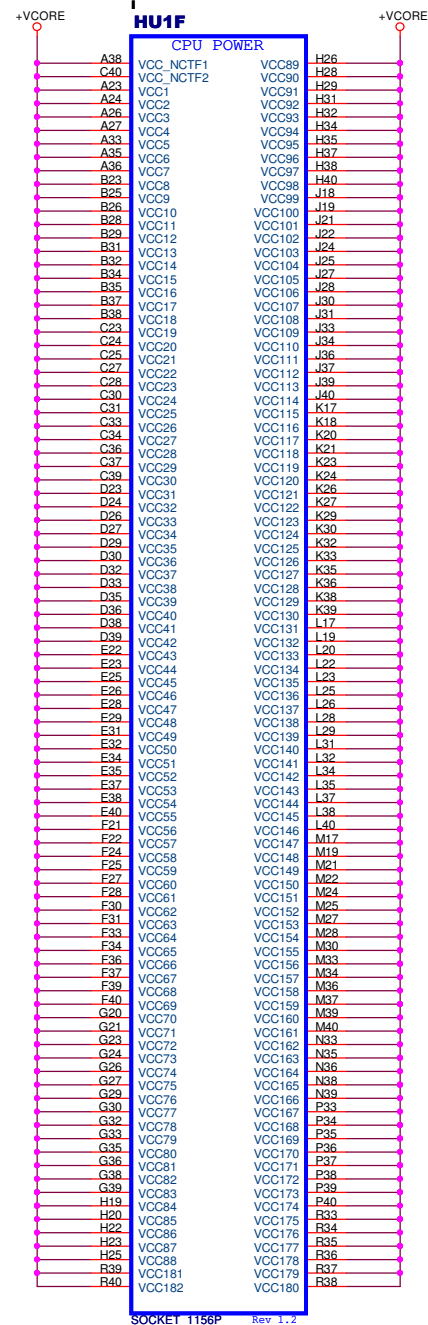
Date: Wednesday, April 07, 2010 Sheet 10 of 68

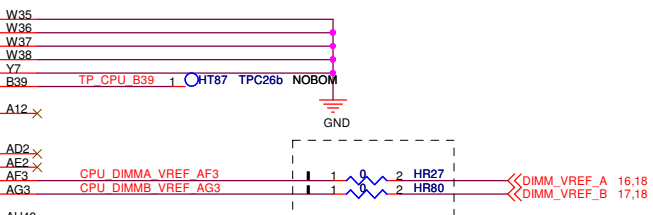
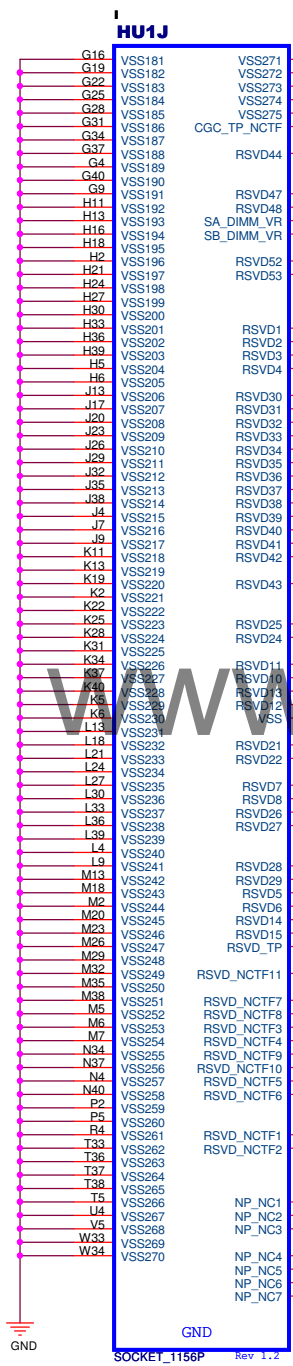
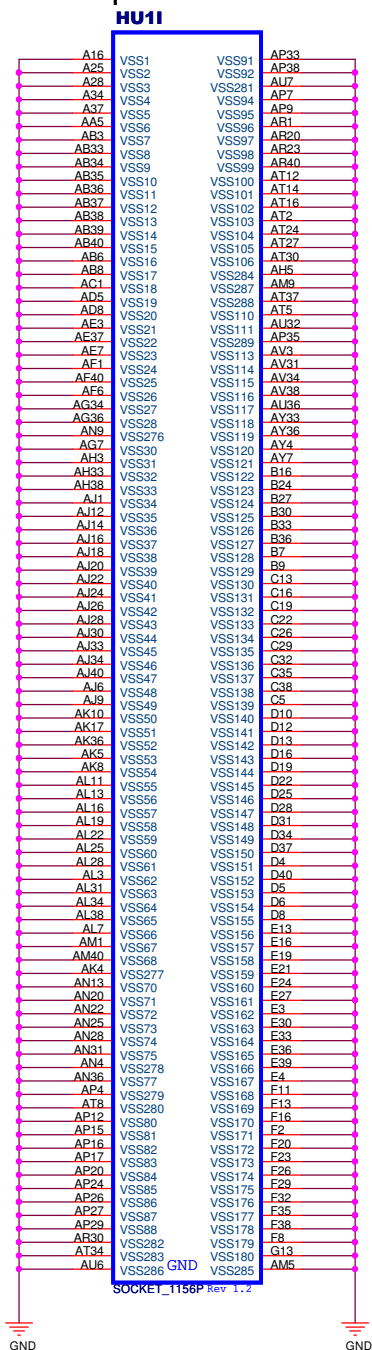










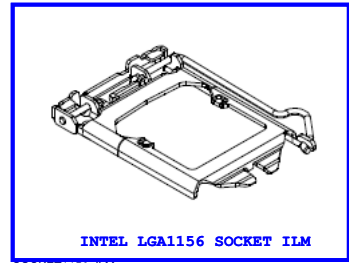


**IHR27 HR80 Change to I for QS CPU**

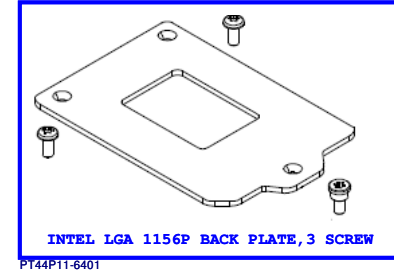
**NOTE:**

Lynnfield	ES2	QS	Production
HR27	NI	I	I
HR80	NI	I	I

**ILM1**



**BACKPLATE1**



**PEGATRON DT-MB RESTRICTED SECRET**

**PEGATRON** Title : CPU 1160 + MEMORY - 6

Pegatron Corp. Engineer: Vic\_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

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**NOTE:**  
Below 4 signals are different connection in Eaglelake DDR3 platform  
Channel A : CS1/WE/MA0  
Channel B : ODT3

XMM1 COLOR: BLUE

XMM1A

M\_CHA\_MAA0 188  
M\_CHA\_MAA1 181  
M\_CHA\_MAA2 61  
M\_CHA\_MAA3 180  
M\_CHA\_MAA4 59  
M\_CHA\_MAA5 58  
M\_CHA\_MAA6 178  
M\_CHA\_MAA7 56  
M\_CHA\_MAA8 177  
M\_CHA\_MAA9 175  
M\_CHA\_MAA10 70  
M\_CHA\_MAA11 55  
M\_CHA\_MAA12 174  
M\_CHA\_MAA13 196  
M\_CHA\_MAA14 172  
M\_CHA\_MAA15 171

A0  
A1  
A2  
A3  
A4  
A5  
A6  
A7  
A8  
A9  
A10/AP  
A11  
A12  
A13  
A14  
A15

D063 234 M\_CHA\_D063  
D062 233 M\_CHA\_D062  
D061 228 M\_CHA\_D061  
D060 227 M\_CHA\_D060  
D059 115 M\_CHA\_D059  
D058 114 M\_CHA\_D058  
D057 109 M\_CHA\_D057  
D056 108 M\_CHA\_D056  
D055 225 M\_CHA\_D055  
D054 224 M\_CHA\_D054  
D053 219 M\_CHA\_D053  
D052 218 M\_CHA\_D052  
D051 106 M\_CHA\_D051  
D050 105 M\_CHA\_D050  
D049 100 M\_CHA\_D049  
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D029 149 M\_CHA\_D029  
D028 148 M\_CHA\_D028  
D027 37 M\_CHA\_D027  
D026 36 M\_CHA\_D026  
D025 31 M\_CHA\_D025  
D024 30 M\_CHA\_D024  
D023 147 M\_CHA\_D023  
D022 146 M\_CHA\_D022  
D021 141 M\_CHA\_D021  
D020 140 M\_CHA\_D020  
D019 28 M\_CHA\_D019  
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D017 22 M\_CHA\_D017  
D016 21 M\_CHA\_D016  
D015 138 M\_CHA\_D015  
D014 137 M\_CHA\_D014  
D013 132 M\_CHA\_D013  
D012 131 M\_CHA\_D012  
D011 19 M\_CHA\_D011  
D010 18 M\_CHA\_D010  
D009 13 M\_CHA\_D009  
D008 12 M\_CHA\_D008  
D007 129 M\_CHA\_D007  
D006 128 M\_CHA\_D006  
D005 123 M\_CHA\_D005  
D004 122 M\_CHA\_D004  
D003 10 M\_CHA\_D003  
D002 9 M\_CHA\_D002  
D001 4 M\_CHA\_D001  
D000 3 M\_CHA\_D000

D063  
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D001  
D000

**NOTE:**

Check clock source if CPU implemented

10 M\_CHA\_CLK1 >> 63  
10 M\_CHA\_CLK1# >> 64  
10 M\_CHA\_CLK0 >> 184  
10 M\_CHA\_CLK0# >> 185

10 M\_CHA\_CS#1 >> 76  
10 M\_CHA\_CS#0 >> 193

10 M\_CHA\_CKE1 >> 169  
10 M\_CHA\_CKE0 >> 50

10 M\_CHA\_BA2 >> 52  
10 M\_CHA\_BA1 >> 190  
10 M\_CHA\_BA0 >> 71

8,17,49,57 SMB\_DATA\_M >> 238  
8,17,49,57 SMB\_CLK\_M >> 118  
10 MA\_ECC\_CB[0..7] >> 165

**NOTE:**

For ECC DIMM

MA\_ECC\_CB7 165  
MA\_ECC\_CB6 164  
MA\_ECC\_CB5 158  
MA\_ECC\_CB4 158  
MA\_ECC\_CB3 140  
MA\_ECC\_CB2 45  
MA\_ECC\_CB1 40  
MA\_ECC\_CB0 39

SA1  
SA0

10 M\_CHA\_WE# >> 73  
10 M\_CHA\_RAS# >> 192  
10 M\_CHA\_CAS# >> 74

10 M\_CHA\_ODT1 >> 77  
10 M\_CHA\_ODT0 >> 195

10,17 DDR3\_DRAMRST# >> 168

RESET#

10 M\_CHA\_DM7 >> 161  
10 M\_CHA\_DM6 >> 230  
10 M\_CHA\_DM5 >> 231  
10 M\_CHA\_DM4 >> 212  
10 M\_CHA\_DM3 >> 213  
10 M\_CHA\_DM2 >> 204  
10 M\_CHA\_DM1 >> 152  
10 M\_CHA\_DM0 >> 143

10 M\_CHA\_DM7 >> 161  
10 M\_CHA\_DM6 >> 230  
10 M\_CHA\_DM5 >> 231  
10 M\_CHA\_DM4 >> 212  
10 M\_CHA\_DM3 >> 213  
10 M\_CHA\_DM2 >> 204  
10 M\_CHA\_DM1 >> 152  
10 M\_CHA\_DM0 >> 143

10 M\_CHA\_DM7 >> 161  
10 M\_CHA\_DM6 >> 230  
10 M\_CHA\_DM5 >> 231  
10 M\_CHA\_DM4 >> 212  
10 M\_CHA\_DM3 >> 213  
10 M\_CHA\_DM2 >> 204  
10 M\_CHA\_DM1 >> 152  
10 M\_CHA\_DM0 >> 143

10 M\_CHA\_DM7 >> 161  
10 M\_CHA\_DM6 >> 230  
10 M\_CHA\_DM5 >> 231  
10 M\_CHA\_DM4 >> 212  
10 M\_CHA\_DM3 >> 213  
10 M\_CHA\_DM2 >> 204  
10 M\_CHA\_DM1 >> 152  
10 M\_CHA\_DM0 >> 143

10 M\_CHA\_DM7 >> 161  
10 M\_CHA\_DM6 >> 230  
10 M\_CHA\_DM5 >> 231  
10 M\_CHA\_DM4 >> 212  
10 M\_CHA\_DM3 >> 213  
10 M\_CHA\_DM2 >> 204  
10 M\_CHA\_DM1 >> 152  
10 M\_CHA\_DM0 >> 143

10 M\_CHA\_DM7 >> 161  
10 M\_CHA\_DM6 >> 230  
10 M\_CHA\_DM5 >> 231  
10 M\_CHA\_DM4 >> 212  
10 M\_CHA\_DM3 >> 213  
10 M\_CHA\_DM2 >> 204  
10 M\_CHA\_DM1 >> 152  
10 M\_CHA\_DM0 >> 143

**NOTE:**

For ECC DIMM

FREE1 198  
FREE2 187  
FREE3 53  
FREE4 48

NC/ERR\_OUT  
NC/TEST4

DDR3\_DIMM\_240P

XMM2 COLOR: BLACK

XMM2A

M\_CHA\_MAA0 188  
M\_CHA\_MAA1 181  
M\_CHA\_MAA2 61  
M\_CHA\_MAA3 180  
M\_CHA\_MAA4 59  
M\_CHA\_MAA5 58  
M\_CHA\_MAA6 178  
M\_CHA\_MAA7 56  
M\_CHA\_MAA8 177  
M\_CHA\_MAA9 175  
M\_CHA\_MAA10 70  
M\_CHA\_MAA11 55  
M\_CHA\_MAA12 174  
M\_CHA\_MAA13 196  
M\_CHA\_MAA14 172  
M\_CHA\_MAA15 171

A0  
A1  
A2  
A3  
A4  
A5  
A6  
A7  
A8  
A9  
A10/AP  
A11  
A12  
A13  
A14  
A15

D063 234 M\_CHA\_D063  
D062 233 M\_CHA\_D062  
D061 228 M\_CHA\_D061  
D060 227 M\_CHA\_D060  
D059 115 M\_CHA\_D059  
D058 114 M\_CHA\_D058  
D057 109 M\_CHA\_D057  
D056 108 M\_CHA\_D056  
D055 225 M\_CHA\_D055  
D054 224 M\_CHA\_D054  
D053 219 M\_CHA\_D053  
D052 218 M\_CHA\_D052  
D051 106 M\_CHA\_D051  
D050 105 M\_CHA\_D050  
D049 100 M\_CHA\_D049  
D048 99 M\_CHA\_D048  
D047 216 M\_CHA\_D047  
D046 215 M\_CHA\_D046  
D045 210 M\_CHA\_D045  
D044 209 M\_CHA\_D044  
D043 97 M\_CHA\_D043  
D042 96 M\_CHA\_D042  
D041 91 M\_CHA\_D041  
D040 207 M\_CHA\_D040  
D039 206 M\_CHA\_D039  
D038 201 M\_CHA\_D038  
D037 200 M\_CHA\_D037  
D036 88 M\_CHA\_D036  
D035 87 M\_CHA\_D035  
D034 82 M\_CHA\_D034  
D033 81 M\_CHA\_D033  
D032 156 M\_CHA\_D032  
D031 155 M\_CHA\_D031  
D030 150 M\_CHA\_D030  
D029 149 M\_CHA\_D029  
D028 148 M\_CHA\_D028  
D027 37 M\_CHA\_D027  
D026 36 M\_CHA\_D026  
D025 31 M\_CHA\_D025  
D024 30 M\_CHA\_D024  
D023 147 M\_CHA\_D023  
D022 146 M\_CHA\_D022  
D021 141 M\_CHA\_D021  
D020 140 M\_CHA\_D020  
D019 28 M\_CHA\_D019  
D018 27 M\_CHA\_D018  
D017 22 M\_CHA\_D017  
D016 21 M\_CHA\_D016  
D015 138 M\_CHA\_D015  
D014 137 M\_CHA\_D014  
D013 132 M\_CHA\_D013  
D012 131 M\_CHA\_D012  
D011 19 M\_CHA\_D011  
D010 18 M\_CHA\_D010  
D009 13 M\_CHA\_D009  
D008 12 M\_CHA\_D008  
D007 129 M\_CHA\_D007  
D006 128 M\_CHA\_D006  
D005 123 M\_CHA\_D005  
D004 122 M\_CHA\_D004  
D003 10 M\_CHA\_D003  
D002 9 M\_CHA\_D002  
D001 4 M\_CHA\_D001  
D000 3 M\_CHA\_D000

D063  
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D007  
D006  
D005  
D004  
D003  
D002  
D001  
D000

**NOTE:**

Check clock source if CPU implemented

10 M\_CHA\_CLK3 >> 63  
10 M\_CHA\_CLK3# >> 64  
10 M\_CHA\_CLK2 >> 184  
10 M\_CHA\_CLK2# >> 185

10 M\_CHA\_CS#3 >> 76  
10 M\_CHA\_CS#2 >> 193

10 M\_CHA\_CKE3 >> 169  
10 M\_CHA\_CKE2 >> 50

10 M\_CHA\_BA2 >> 52  
10 M\_CHA\_BA1 >> 190  
10 M\_CHA\_BA0 >> 71

8,17,49,57 SMB\_DATA\_M >> 238  
8,17,49,57 SMB\_CLK\_M >> 118  
10 MA\_ECC\_CB[0..7] >> 165

**NOTE:**

For ECC DIMM

MA\_ECC\_CB7 165  
MA\_ECC\_CB6 164  
MA\_ECC\_CB5 158  
MA\_ECC\_CB4 158  
MA\_ECC\_CB3 140  
MA\_ECC\_CB2 45  
MA\_ECC\_CB1 40  
MA\_ECC\_CB0 39

SA1  
SA0

10 M\_CHA\_WE# >> 73  
10 M\_CHA\_RAS# >> 192  
10 M\_CHA\_CAS# >> 74

10 M\_CHA\_ODT3 >> 77  
10 M\_CHA\_ODT2 >> 195

10,17 DDR3\_DRAMRST# >> 168

RESET#

10 M\_CHA\_DM7 >> 161  
10 M\_CHA\_DM6 >> 230  
10 M\_CHA\_DM5 >> 231  
10 M\_CHA\_DM4 >> 212  
10 M\_CHA\_DM3 >> 213  
10 M\_CHA\_DM2 >> 204  
10 M\_CHA\_DM1 >> 152  
10 M\_CHA\_DM0 >> 143

10 M\_CHA\_DM7 >> 161  
10 M\_CHA\_DM6 >> 230  
10 M\_CHA\_DM5 >> 231  
10 M\_CHA\_DM4 >> 212  
10 M\_CHA\_DM3 >> 213  
10 M\_CHA\_DM2 >> 204  
10 M\_CHA\_DM1 >> 152  
10 M\_CHA\_DM0 >> 143

10 M\_CHA\_DM7 >> 161  
10 M\_CHA\_DM6 >> 230  
10 M\_CHA\_DM5 >> 231  
10 M\_CHA\_DM4 >> 212  
10 M\_CHA\_DM3 >> 213  
10 M\_CHA\_DM2 >> 204  
10 M\_CHA\_DM1 >> 152  
10 M\_CHA\_DM0 >> 143

10 M\_CHA\_DM7 >> 161  
10 M\_CHA\_DM6 >> 230  
10 M\_CHA\_DM5 >> 231  
10 M\_CHA\_DM4 >> 212  
10 M\_CHA\_DM3 >> 213  
10 M\_CHA\_DM2 >> 204  
10 M\_CHA\_DM1 >> 152  
10 M\_CHA\_DM0 >> 143

10 M\_CHA\_DM7 >> 161  
10 M\_CHA\_DM6 >> 230  
10 M\_CHA\_DM5 >> 231  
10 M\_CHA\_DM4 >> 212  
10 M\_CHA\_DM3 >> 213  
10 M\_CHA\_DM2 >> 204  
10 M\_CHA\_DM1 >> 152  
10 M\_CHA\_DM0 >> 143

10 M\_CHA\_DM7 >> 161  
10 M\_CHA\_DM6 >> 230  
10 M\_CHA\_DM5 >> 231  
10 M\_CHA\_DM4 >> 212  
10 M\_CHA\_DM3 >> 213  
10 M\_CHA\_DM2 >> 204  
10 M\_CHA\_DM1 >> 152  
10 M\_CHA\_DM0 >> 143

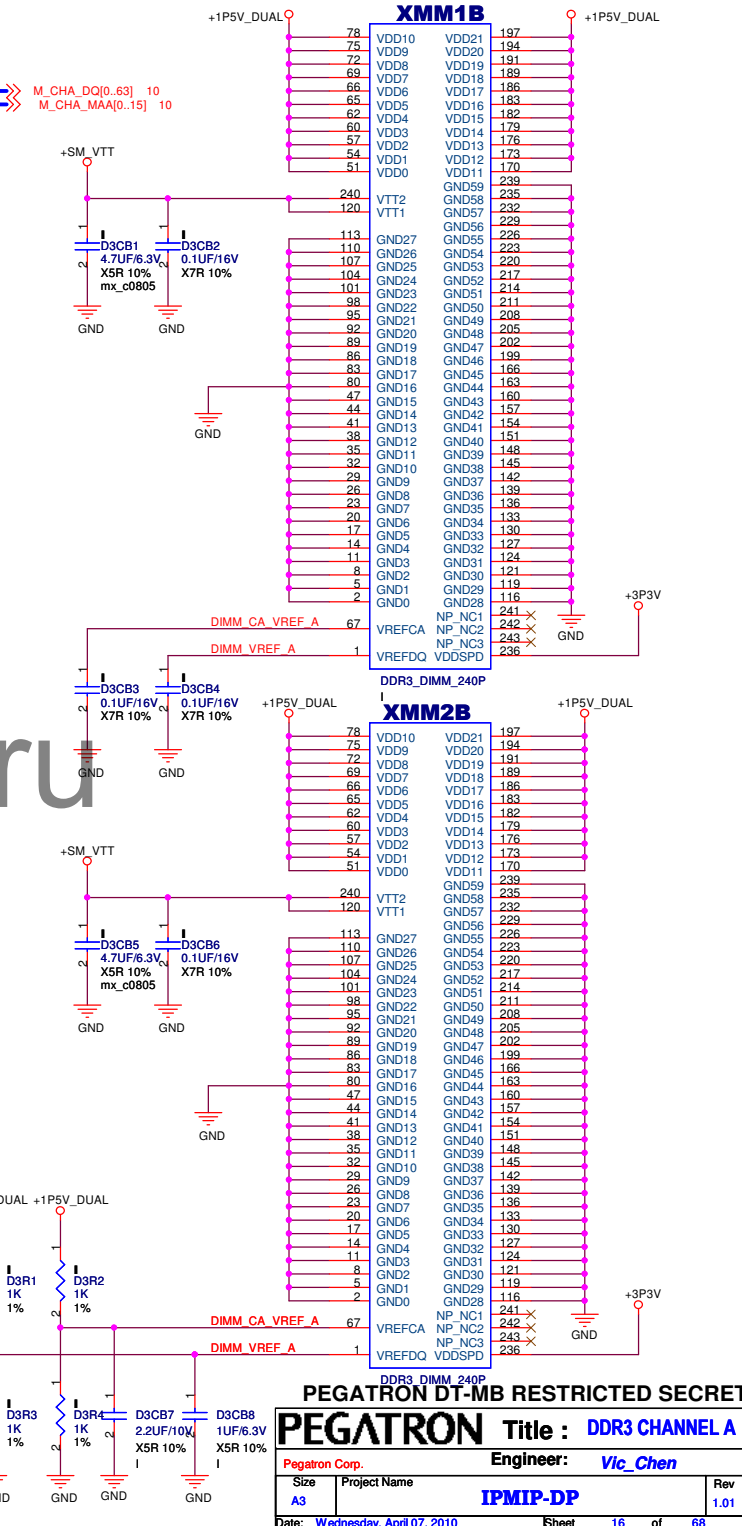
**NOTE:**

For ECC DIMM

FREE1 198  
FREE2 187  
FREE3 53  
FREE4 48

NC/ERR\_OUT  
NC/TEST4

DDR3\_DIMM\_240P





XMM3 COLOR: BLUE

### XMM3A

M_CHB_MAA0	188	A0	DQ63	234	M_CHB_DQ63
M_CHB_MAA1	181	A1	DQ62	233	M_CHB_DQ62
M_CHB_MAA2	61	A2	DQ61	228	M_CHB_DQ61
M_CHB_MAA3	180	A3	DQ60	227	M_CHB_DQ60
M_CHB_MAA4	59	A4	DQ59	114	M_CHB_DQ59
M_CHB_MAA5	58	A5	DQ58	109	M_CHB_DQ58
M_CHB_MAA6	178	A6	DQ57	108	M_CHB_DQ57
M_CHB_MAA7	56	A7	DQ56	225	M_CHB_DQ56
M_CHB_MAA8	177	A8	DQ55	224	M_CHB_DQ55
M_CHB_MAA9	175	A9	DQ54	219	M_CHB_DQ54
M_CHB_MAA10	70	A10/AP	DQ53	218	M_CHB_DQ53
M_CHB_MAA11	55	A11	DQ52	106	M_CHB_DQ52
M_CHB_MAA12	174	A12	DQ51	105	M_CHB_DQ51
M_CHB_MAA13	196	A13	DQ50	100	M_CHB_DQ50
M_CHB_MAA14	172	A14	DQ49	99	M_CHB_DQ49
M_CHB_MAA15	171	A15	DQ48	216	M_CHB_DQ48

**NOTE:**  
Check clock source if CPU  
implemented

M_CHB_CLK1#	63	CK1P/NU	DQ47	215	M_CHB_DQ47
M_CHB_CLK1#	184	CK1N/NU	DQ46	210	M_CHB_DQ46
M_CHB_CLK0#	185	CK0P	DQ45	209	M_CHB_DQ45
M_CHB_CLK0#	185	CK0N	DQ44	97	M_CHB_DQ44

M_CHB_CS#1	76	CS1#	DQ43	96	M_CHB_DQ43
M_CHB_CS#0	193	CS0#	DQ42	97	M_CHB_DQ42
M_CHB_CKE1	169	CKE1	DQ41	91	M_CHB_DQ41
M_CHB_CKE0	50	CKE0	DQ40	90	M_CHB_DQ40
M_CHB_BA2	50	BA2	DQ39	207	M_CHB_DQ39
M_CHB_BA1	71	BA1	DQ38	206	M_CHB_DQ38
M_CHB_BA0	71	BA0	DQ37	201	M_CHB_DQ37

SMB DATA_M	238	SDA	DQ36	200	M_CHB_DQ36
SMB CLK_M	118	SCL	DQ35	88	M_CHB_DQ35
MB_ECC_CB[0..7]	165	CB7	DQ34	87	M_CHB_DQ34

MB_ECC_CB6	164	CB6	DQ33	82	M_CHB_DQ33
MB_ECC_CB5	159	CB5	DQ32	81	M_CHB_DQ32
MB_ECC_CB4	158	CB4	DQ31	156	M_CHB_DQ31
MB_ECC_CB3	46	CB3	DQ30	155	M_CHB_DQ30
MB_ECC_CB2	45	CB2	DQ29	150	M_CHB_DQ29
MB_ECC_CB1	40	CB1	DQ28	149	M_CHB_DQ28
MB_ECC_CB0	39	CB0	DQ27	37	M_CHB_DQ27

SA1	237	SA1	DQ26	36	M_CHB_DQ26
SA0	117	SA0	DQ25	31	M_CHB_DQ25

WE#	73	WE#	DQ24	147	M_CHB_DQ24
RAS#	192	RAS#	DQ23	146	M_CHB_DQ23
CAS#	74	CAS#	DQ22	141	M_CHB_DQ22

ODT1	77	ODT1	DQ21	140	M_CHB_DQ21
ODT0	195	ODT0	DQ20	139	M_CHB_DQ20

RESET#	168	RESET#	DQ19	27	M_CHB_DQ19
RESET#	168	RESET#	DQ18	22	M_CHB_DQ18

DM8/DQS17P	161	DM8/DQS17P	DQ17	21	M_CHB_DQ17
DM7/DQS16P	230	DM7/DQS16P	DQ16	138	M_CHB_DQ16

DM6/DQS15P	231	DM6/DQS15P	DQ15	137	M_CHB_DQ15
DM5/DQS14P	232	DM5/DQS14P	DQ14	132	M_CHB_DQ14

DM4/DQS13P	233	DM4/DQS13P	DQ13	131	M_CHB_DQ13
DM3/DQS12P	234	DM3/DQS12P	DQ12	19	M_CHB_DQ12

DM2/DQS11P	235	DM2/DQS11P	DQ11	18	M_CHB_DQ11
DM1/DQS10P	236	DM1/DQS10P	DQ10	13	M_CHB_DQ10

DM0/DQS9P	237	DM0/DQS9P	DQ9	12	M_CHB_DQ9
DM0/DQS8P	238	DM0/DQS8P	DQ8	129	M_CHB_DQ8

DM0/DQS7P	239	DM0/DQS7P	DQ7	128	M_CHB_DQ7
DM0/DQS6P	240	DM0/DQS6P	DQ6	127	M_CHB_DQ6

DM0/DQS5P	241	DM0/DQS5P	DQ5	126	M_CHB_DQ5
DM0/DQS4P	242	DM0/DQS4P	DQ4	125	M_CHB_DQ4

DM0/DQS3P	243	DM0/DQS3P	DQ3	124	M_CHB_DQ3
DM0/DQS2P	244	DM0/DQS2P	DQ2	123	M_CHB_DQ2

DM0/DQS1P	245	DM0/DQS1P	DQ1	4	M_CHB_DQ1
DM0/DQS0P	246	DM0/DQS0P	DQ0	3	M_CHB_DQ0

DM0/DQS0P	247	DM0/DQS0P	DQ0	3	M_CHB_DQ0
DM0/DQS0P	248	DM0/DQS0P	DQ0	3	M_CHB_DQ0

DM0/DQS0P	249	DM0/DQS0P	DQ0	3	M_CHB_DQ0
DM0/DQS0P	250	DM0/DQS0P	DQ0	3	M_CHB_DQ0

XMM4 COLOR: BLACK

### XMM4A

M_CHB_MAA0	188	A0	DQ63	234	M_CHB_DQ63
M_CHB_MAA1	181	A1	DQ62	233	M_CHB_DQ62
M_CHB_MAA2	61	A2	DQ61	228	M_CHB_DQ61
M_CHB_MAA3	180	A3	DQ60	227	M_CHB_DQ60
M_CHB_MAA4	59	A4	DQ59	114	M_CHB_DQ59
M_CHB_MAA5	58	A5	DQ58	109	M_CHB_DQ58
M_CHB_MAA6	178	A6	DQ57	108	M_CHB_DQ57
M_CHB_MAA7	56	A7	DQ56	225	M_CHB_DQ56
M_CHB_MAA8	177	A8	DQ55	224	M_CHB_DQ55
M_CHB_MAA9	175	A9	DQ54	219	M_CHB_DQ54
M_CHB_MAA10	70	A10/AP	DQ53	218	M_CHB_DQ53
M_CHB_MAA11	55	A11	DQ52	106	M_CHB_DQ52
M_CHB_MAA12	174	A12	DQ51	105	M_CHB_DQ51
M_CHB_MAA13	196	A13	DQ50	100	M_CHB_DQ50
M_CHB_MAA14	172	A14	DQ49	99	M_CHB_DQ49
M_CHB_MAA15	171	A15	DQ48	216	M_CHB_DQ48

**NOTE:**  
Check clock source if CPU  
implemented

M_CHB_CLK1#	63	CK1P/NU	DQ47	215	M_CHB_DQ47
M_CHB_CLK1#	184	CK1N/NU	DQ46	210	M_CHB_DQ46
M_CHB_CLK0#	185	CK0P	DQ45	209	M_CHB_DQ45
M_CHB_CLK0#	185	CK0N	DQ44	97	M_CHB_DQ44

M_CHB_CS#1	76	CS1#	DQ43	96	M_CHB_DQ43
M_CHB_CS#0	193	CS0#	DQ42	97	M_CHB_DQ42
M_CHB_CKE1	169	CKE1	DQ41	91	M_CHB_DQ41
M_CHB_CKE0	50	CKE0	DQ40	90	M_CHB_DQ40
M_CHB_BA2	50	BA2	DQ39	207	M_CHB_DQ39
M_CHB_BA1	71	BA1	DQ38	206	M_CHB_DQ38
M_CHB_BA0	71	BA0	DQ37	201	M_CHB_DQ37

SMB DATA_M	238	SDA	DQ36	200	M_CHB_DQ36
SMB CLK_M	118	SCL	DQ35	88	M_CHB_DQ35
MB_ECC_CB[0..7]	165	CB7	DQ34	87	M_CHB_DQ34

MB_ECC_CB6	164	CB6	DQ33	82	M_CHB_DQ33
MB_ECC_CB5	159	CB5	DQ32	81	M_CHB_DQ32
MB_ECC_CB4	158	CB4	DQ31	156	M_CHB_DQ31
MB_ECC_CB3	46	CB3	DQ30	155	M_CHB_DQ30
MB_ECC_CB2	45	CB2	DQ29	150	M_CHB_DQ29
MB_ECC_CB1	40	CB1	DQ28	149	M_CHB_DQ28
MB_ECC_CB0	39	CB0	DQ27	37	M_CHB_DQ27

SA1	237	SA1	DQ26	36	M_CHB_DQ26
SA0	117	SA0	DQ25	31	M_CHB_DQ25

WE#	73	WE#	DQ24	147	M_CHB_DQ24
RAS#	192	RAS#	DQ23	146	M_CHB_DQ23
CAS#	74	CAS#	DQ22	141	M_CHB_DQ22

ODT1	77	ODT1	DQ21	140	M_CHB_DQ21
ODT0	195	ODT0	DQ20	139	M_CHB_DQ20

RESET#	168	RESET#	DQ19	27	M_CHB_DQ19
RESET#	168	RESET#	DQ18	22	M_CHB_DQ18

DM8/DQS17P	161	DM8/DQS17P	DQ17	21	M_CHB_DQ17
DM7/DQS16P	230	DM7/DQS16P	DQ16	138	M_CHB_DQ16

DM6/DQS15P	231	DM6/DQS15P	DQ15	137	M_CHB_DQ15
DM5/DQS14P	232	DM5/DQS14P	DQ14	132	M_CHB_DQ14

DM4/DQS13P	233	DM4/DQS13P	DQ13	131	M_CHB_DQ13
DM3/DQS12P	234	DM3/DQS12P	DQ12	19	M_CHB_DQ12

DM2/DQS11P	235	DM2/DQS11P	DQ11	18	M_CHB_DQ11
DM1/DQS10P	236	DM1/DQS10P	DQ10	13	M_CHB_DQ10

DM0/DQS9P	237	DM0/DQS9P	DQ9	12	M_CHB_DQ9
DM0/DQS8P	238	DM0/DQS8P	DQ8	129	M_CHB_DQ8

DM0/DQS7P	239	DM0/DQS7P	DQ7	128	M_CHB_DQ7
DM0/DQS6P	240	DM0/DQS6P	DQ6	127	M_CHB_DQ6

DM0/DQS5P	241	DM0/DQS5P	DQ5	126	M_CHB_DQ5
DM0/DQS4P	242	DM0/DQS4P	DQ4	125	M_CHB_DQ4

DM0/DQS3P	243	DM0/DQS3P	DQ3	124	M_CHB_DQ3
DM0/DQS2P	244	DM0/DQS2P	DQ2	123	M_CHB_DQ2

DM0/DQS1P	245	DM0/DQS1P	DQ1	4	M_CHB_DQ1
DM0/DQS0P	246	DM0/DQS0P	DQ0	3	M_CHB_DQ0

DM0/DQS0P	247	DM0/DQS0P	DQ0	3	M_CHB_DQ0
DM0/DQS0P	248	DM0/DQS0P	DQ0	3	M_CHB_DQ0

DM0/DQS0P	249	DM0/DQS0P	DQ0	3	M_CHB_DQ0
DM0/DQS0P	250	DM0/DQS0P	DQ0	3	M_CHB_DQ0

M\_CHB\_DQ[0..63] 11  
M\_CHB\_MAA[0..15] 11

+SM\_VTT

+1P5V\_DUAL

+1P5V\_DUAL

+1P5V\_DUAL

+1P5V\_DUAL

+1P5V\_DUAL

+1P5V\_DUAL

+1P5V\_DUAL

+1P5V\_DUAL

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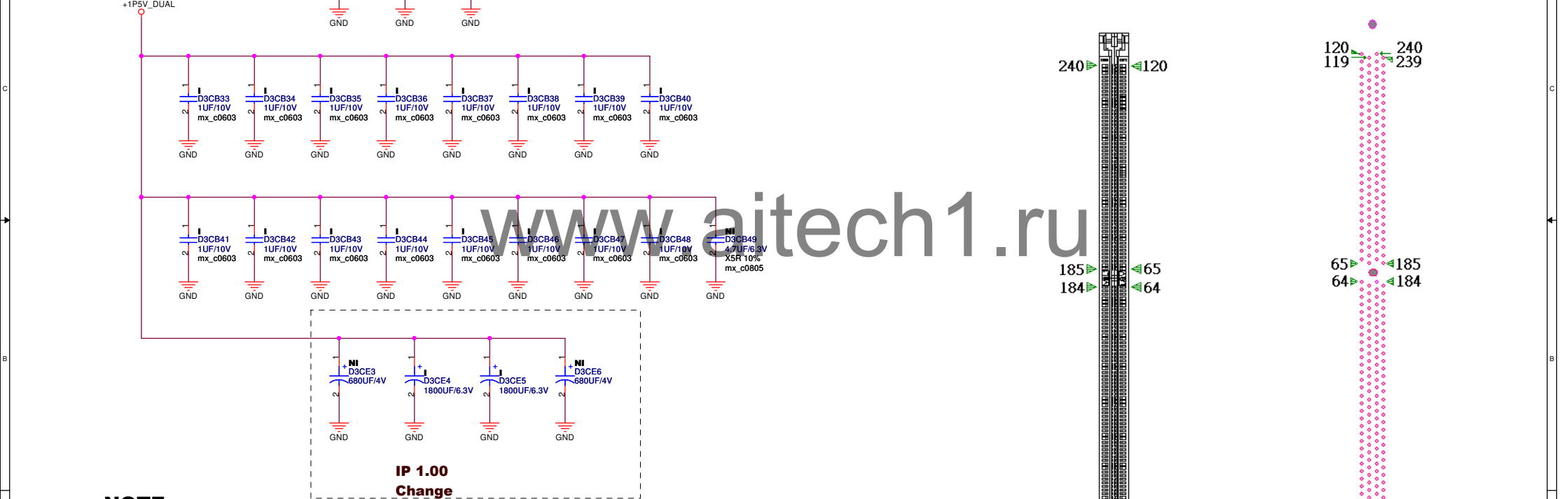
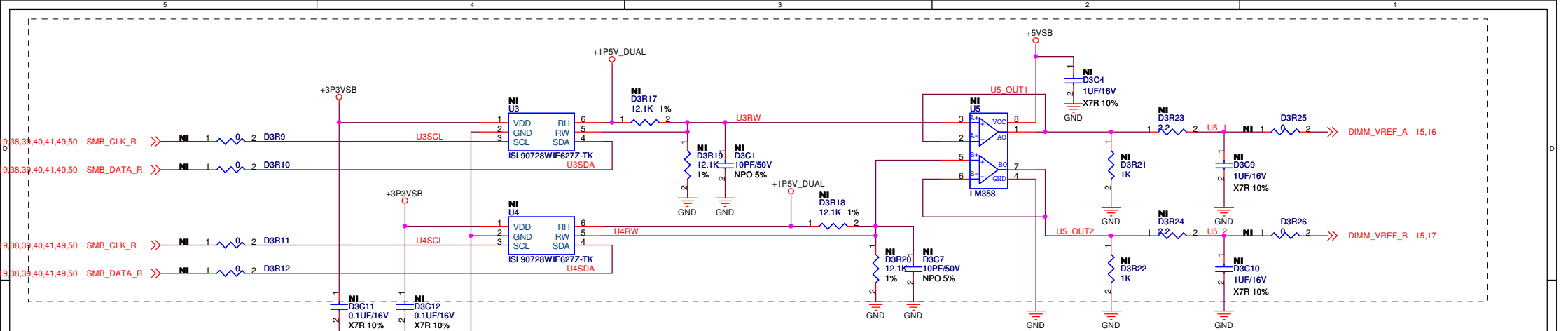
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+1P5V\_DUAL

+1P5V\_DUAL

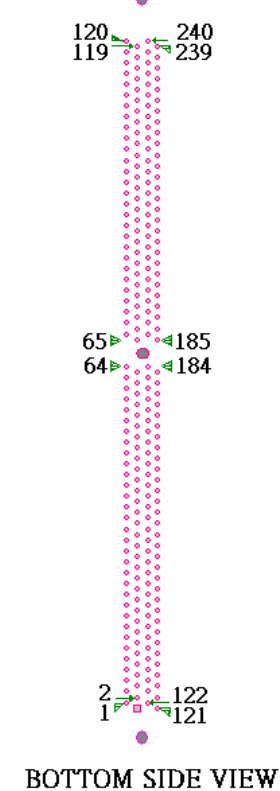
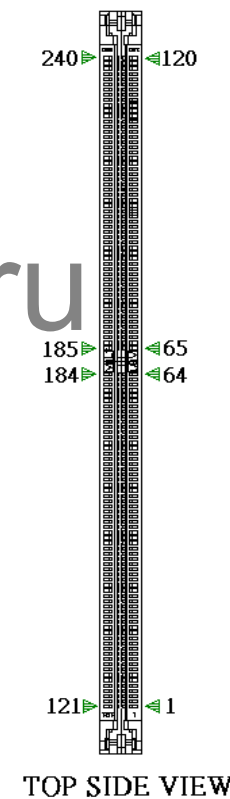
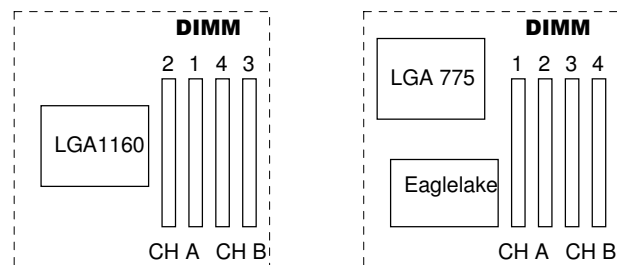
### XMM3B

VDD10	197	VDD21	197
VDD9	194	VDD20	191
VDD8	191	VDD19	189
VDD7	189	VDD18	186
VDD6	186	VDD17	183
VDD5	183	VDD16	180
VDD4	180	VDD15	177
VDD3	177	VDD14	174
VDD2	174	VDD13	171
VDD1	171	VDD12	168
VDD0	168	VDD11	1



# NOTE:

**DIMM Placement for different platform**



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : **DDR3 DECOUPLING**

Pegatron Corp. Engineer: **Vic\_Chen**

Size A3 Project Name **IPMIP-DP** Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 18 of 68

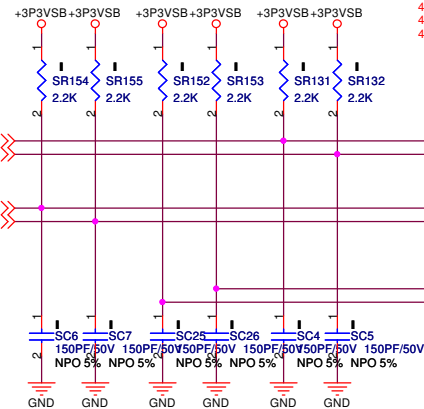
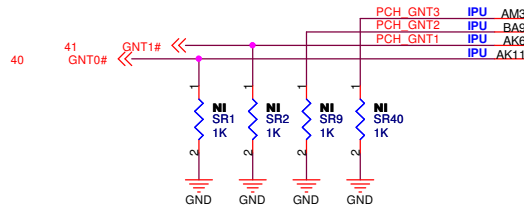
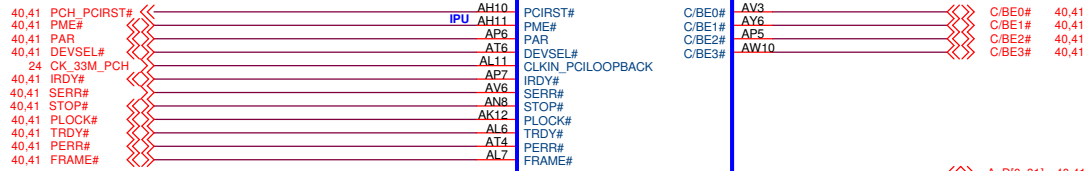
### Strap

(GNT0#~GNT3# have IPU)

GNT3#		
0	TOP Block SWAP	
1	Normal (Default)	

GNT2#		ESI mode (Server Only)
0		DMI (Default)
1		

GNT1#	GNT0#	BOOT BIOS
1	0	RESERVED
0	1	PCI
1	1	SPI
0	0	LPC

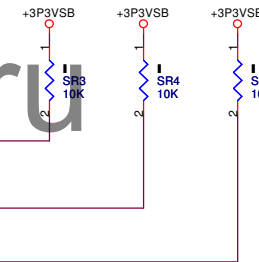


18,38,39,40,41,49,50 SMB\_CLK\_R  
18,38,39,40,41,49,50 SMB\_DATA\_R

36 SML0\_LAN\_CLK  
36 SML0\_LAN\_DATA

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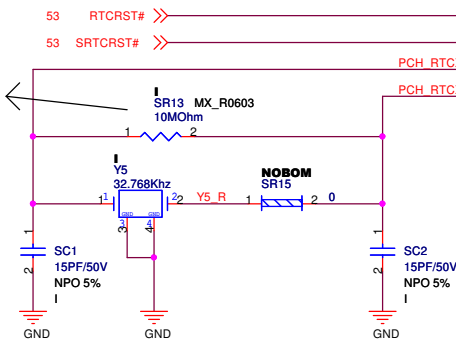
SMBUS



### Strap

SPI_MOSI (IPD)		Disable ITPM (Default)
0		Enable ITPM
1		

CRB R1.0 (page.39) suggests that don't change it to 0402 package type



RTC

SPI

IBEXPEAK Rev 1.0

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL\_PCH - 1

Pegatron Corp. Engineer: Vic\_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Thursday, April 08, 2010

Sheet 19 of 68





Install SR32, SR68, NI SR26 if M3 support  
Install SR26, SR68, NI SR32 if no M3 support



**NOTE:**  
THE TRACES TOGETHER CLOSE TO  
PINS WITH LENGTH NO LONGER THAN  
200 MILS TO RESISTOR

**NOTE:**  
INIT3\_3V# is reserved  
for Strap cpu output  
stronger if low.

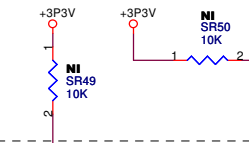
**NOTE:**  
Check if Signal A20GATE, KBDRST#, SERIRQ have a PU resistor in SIO side

NOTE: EDS_Rev2_1 add H55 AHCI support.					
Feature Set	SKU				
	Q57	H57	H55	P55	P57
LVDS	NO	NO	NO	NO	NO
PAVP 1.5	YES	YES	YES	NO	NO
FIS Based Port Multiplier Support	YES	YES	NO	YES	YES
QST	YES	YES	YES	NO	YES
Braidwood	YES	YES	NO	NO	YES
Coral Harbor	NO	NO	NO	NO	YES
AHCI	YES	YES	YES	YES	YES
Raid 0/1/5/10	YES	YES	NO	YES	YES
Ignition ME FW only	NO	NO	NO	YES	NO
AT-p	YES	NO	NO	NO	NO
iAMT 6.0	YES	NO	NO	NO	NO
IRPA for Business	YES	NO	NO	NO	NO
IRPA for Consumer	NO	YES	NO	NO	NO
IRWT	NO	YES	YES	NO	NO

**PEGATRON** Title : INTEL\_PCH-3

Size <b>A3</b>	Project Name <b>IPMIP-DP</b>	Rev <b>1.01</b>
-------------------	---------------------------------	--------------------

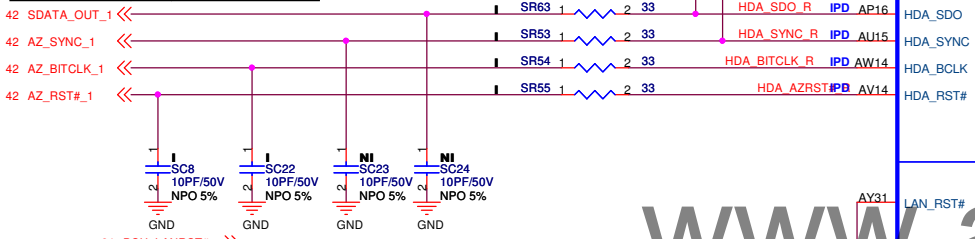
NOTE:  
Internal Pull-up in PCH



### Strap

AZ_DATA_OUT (IPD)	0	1
0	USING CORE POWER FOR NAND FLASH	USING EPW POWER FOR NAND FLASH

AZ_SYNC (IPD)	0	1
0	OnDie PLL VR USE 1.8V SUPPLY	OnDie PLL VR USE 1.5V SUPPLY



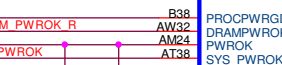
21 PCH\_LANRST#

NOTE:

Install for non-Intel LAN support

13,36,47,50,57 PLTRST#  
8,13,52,57 SYS RESET#  
54 RSMRST#

### IPMIP-GS ADD SC35



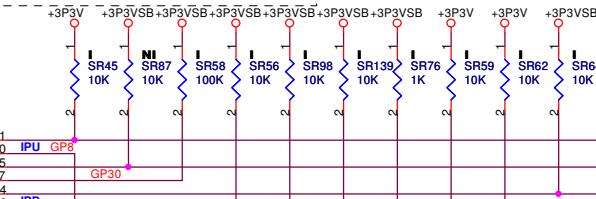
### Strap

INTVRMEN	0	1
0	Disable intergrated 1.05V VRM for GbE	Enable (Default)

### Strap

SPKR (IPD)	0	1
0	Disable No-reboot option	Enable No-reboot option

### SR87 NI for power sequence t237



GPIO33	ME update
1-2	OVERRIDE
2-3	DEFAULT

### JE50:23



### Strap

GPIO8 (IPU)	0	1
0	Chip ENABLE	Chip DISABLE
GPIO15 (IPD)	0	1
0	TLS CONFIDENTIALITY DISABLE	TLS CONFIDENTIALITY ENABLE
GPIO27 (IPU)	0	1
0	OnDie PLL VccVRM DISABLE	OnDie PLL VccVRM ENABLE
GPIO33	0	1
0	Flash descriptor overriden	Flash descriptor in effect

NOTE:  
Just for measure

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL\_PCH - 4

Pegatron Corp. Engineer: Vic\_Chen

Size A3 Project Name IPMIP-DP Rev 1.01

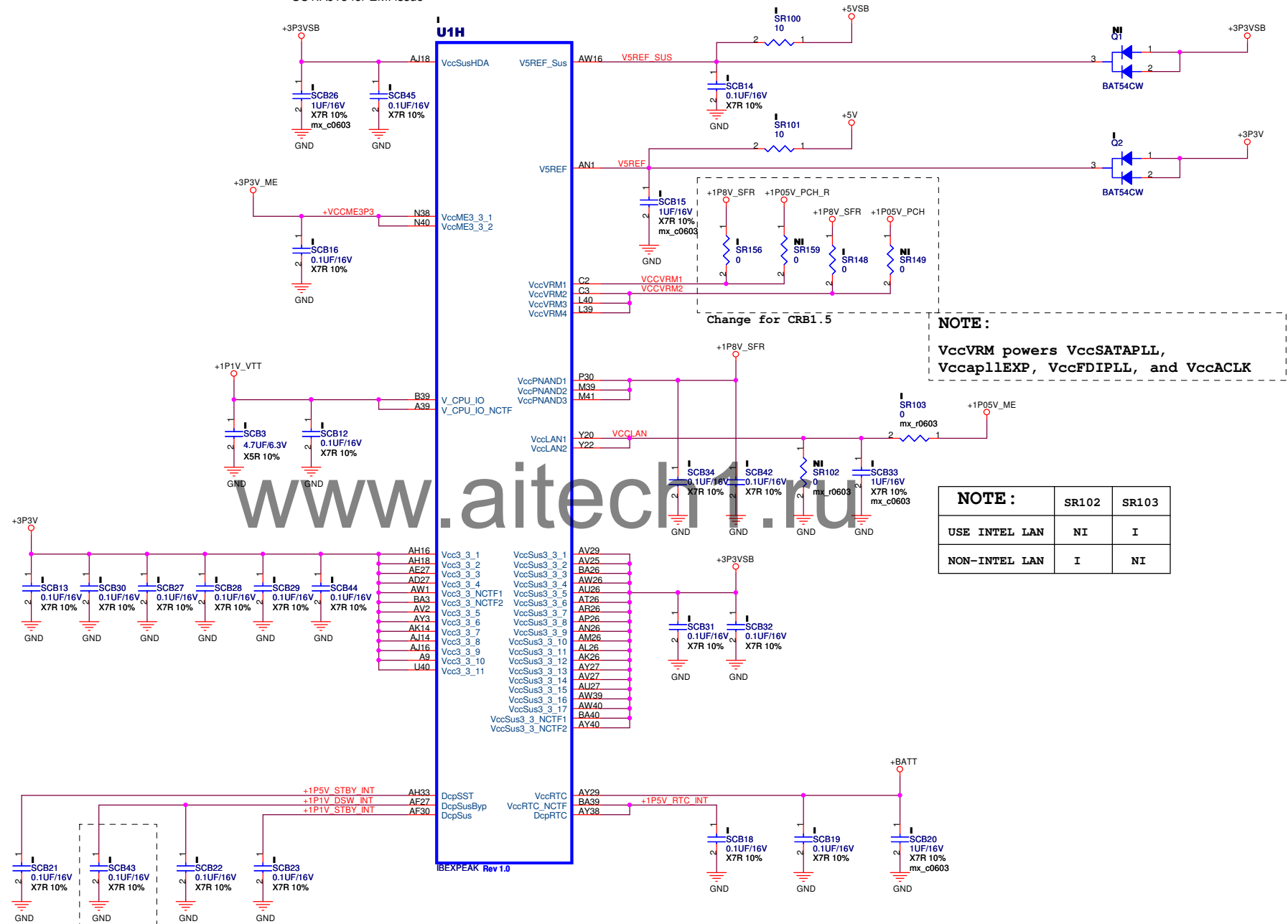
Date: Wednesday, April 07, 2010 Sheet 22 of 68







**Note**  
Place SCB45 close to  
SU1.AJ18 for EMI issue



**NOTE:**  
VccVRM powers VccSATAPLL,  
Vccap11EXP, VccFDIPLL, and VccACLK

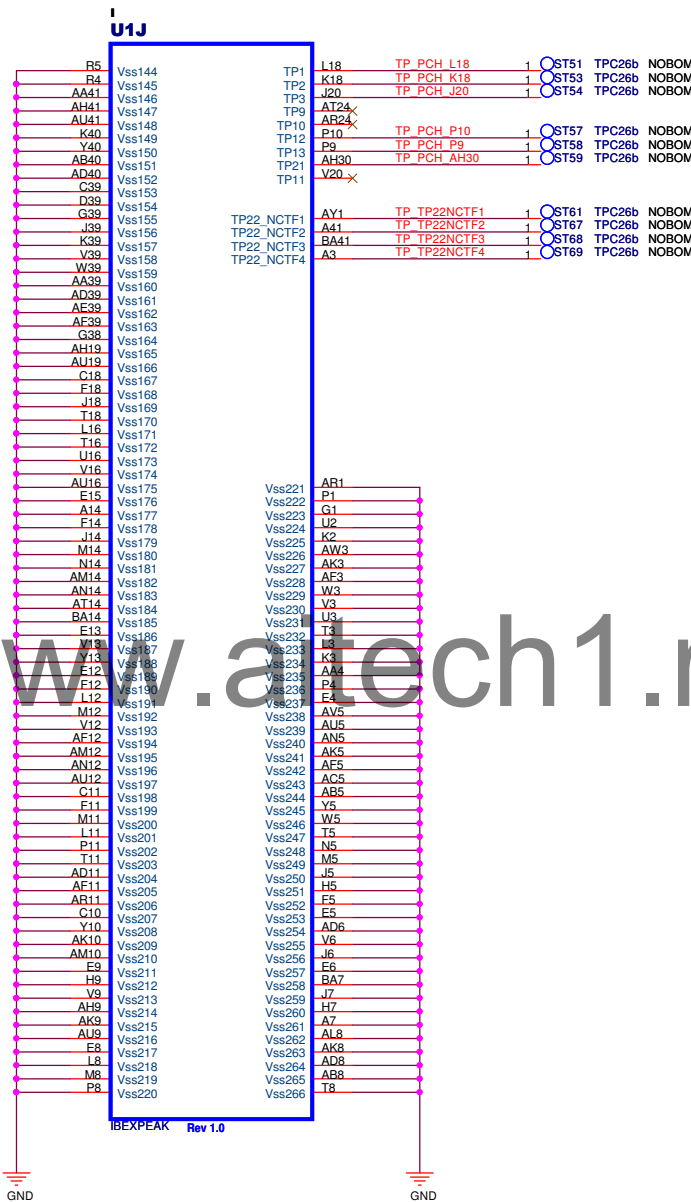
NOTE :	SR102	SR103
USE INTEL LAN	NI	I
NON-INTEL LAN	I	NI

**NOTE:**  
MOW WW08 recommend to  
reserved SCB43.

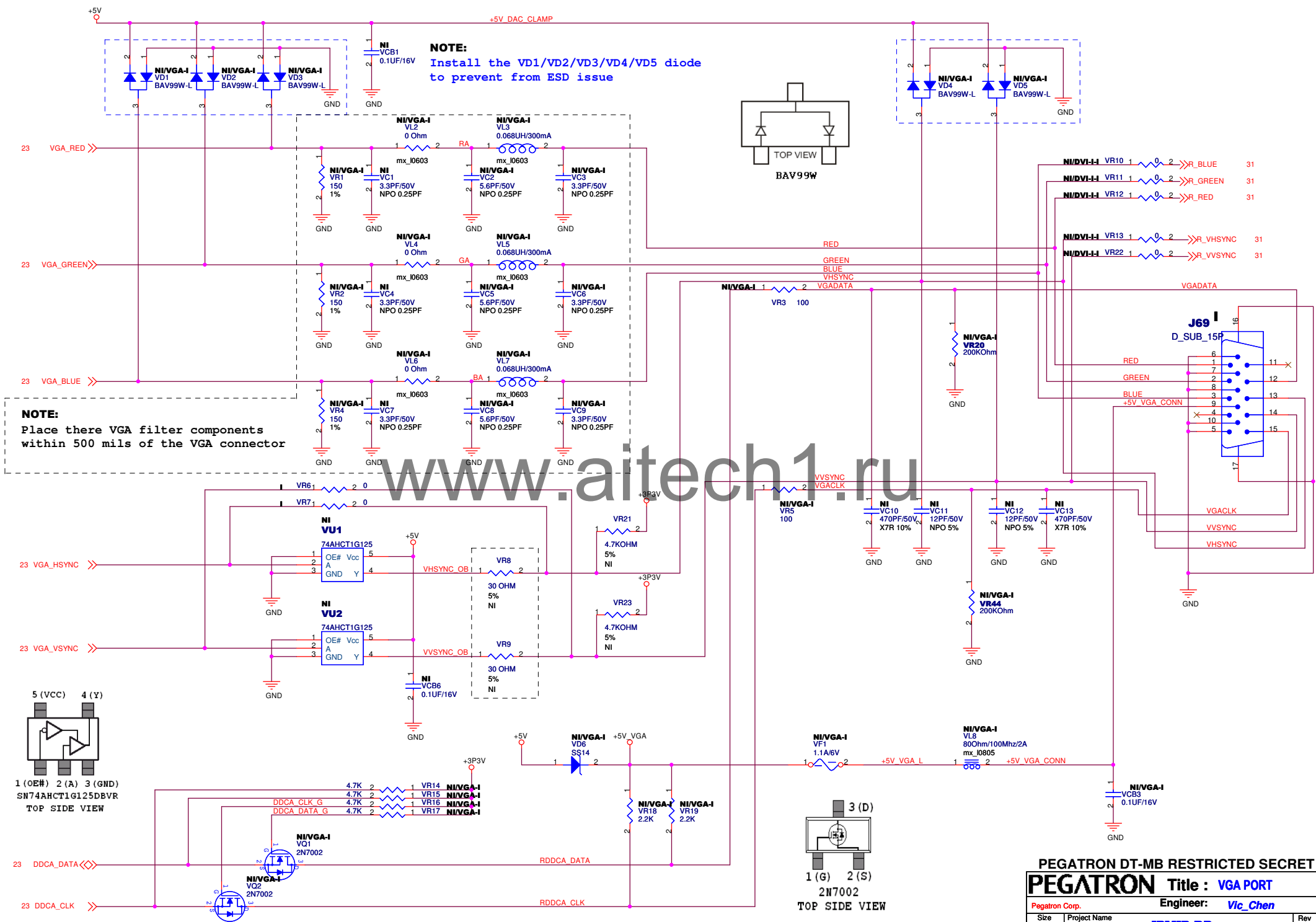
PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : INTEL\_PCH - 8  
Pegatron Corp. Engineer: Vic\_Chen

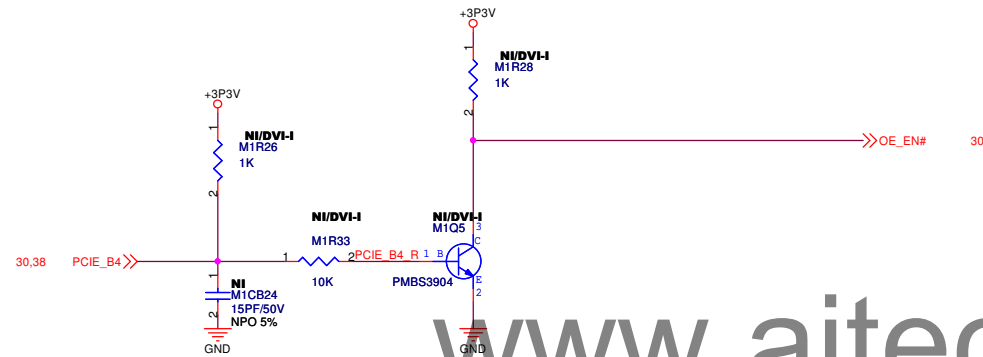
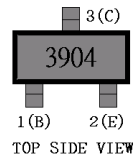
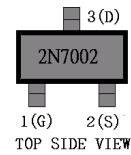
Size	Project Name	Rev
A3	IPMIP-DP	1.01
Date: Tuesday, March 23, 2010	Sheet 26 of 68	











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**NOTE:**

PCIE X16	PCIE_B4	SEL (MUX)	DDC_EN# (Level Shifter)	OE_EN# (Level Shifter)	Function
Plugged	LOW	LOW	LOW	HI	PCIE x16
Unplugged	HI	HI	HI	LOW	DVI , HDMI

PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : DVI Control

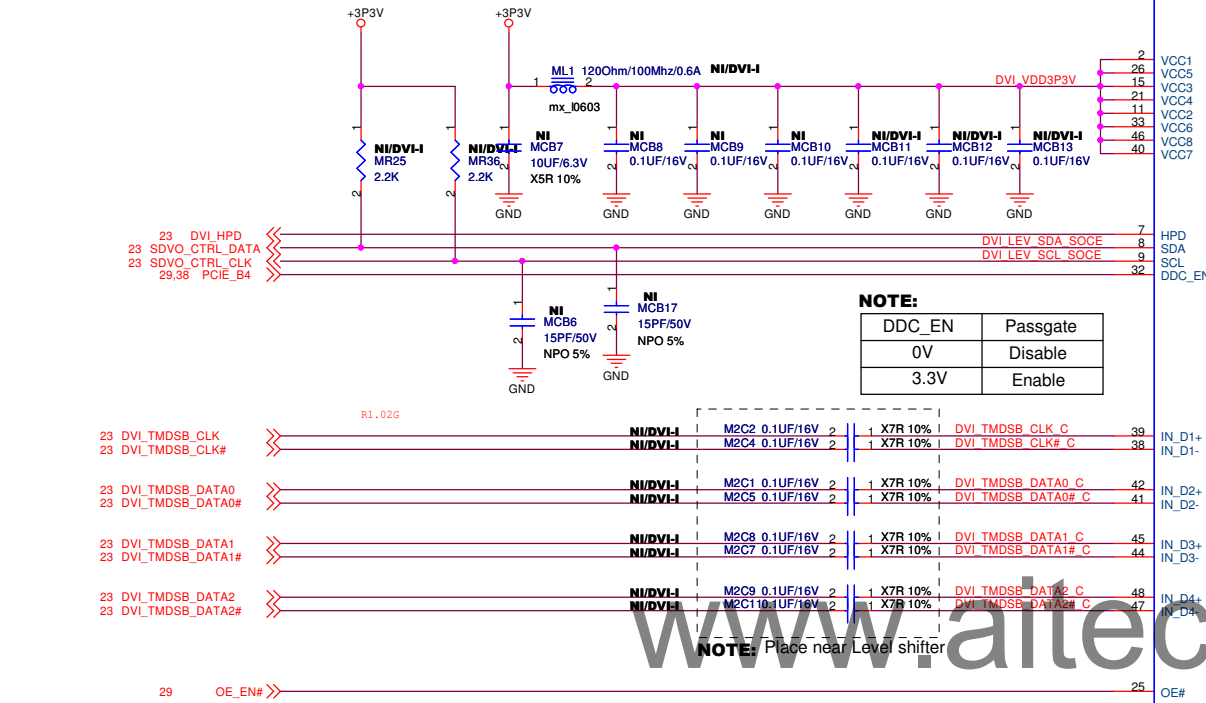
Pegatron Corp. Engineer: Vic\_Chen

Size A3	Project Name IPMIP-DP	Rev 1.01
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Date: Wednesday, April 07, 2010 Sheet 29 of 68

CH7318: 02G480001000  
ASM1442: 022U-0004000

MU5



NOTE: Pericom PI3VDP411LS

Pin 3, 4, 6, 10, 34, and 35 are internal 100K ohm pull-up

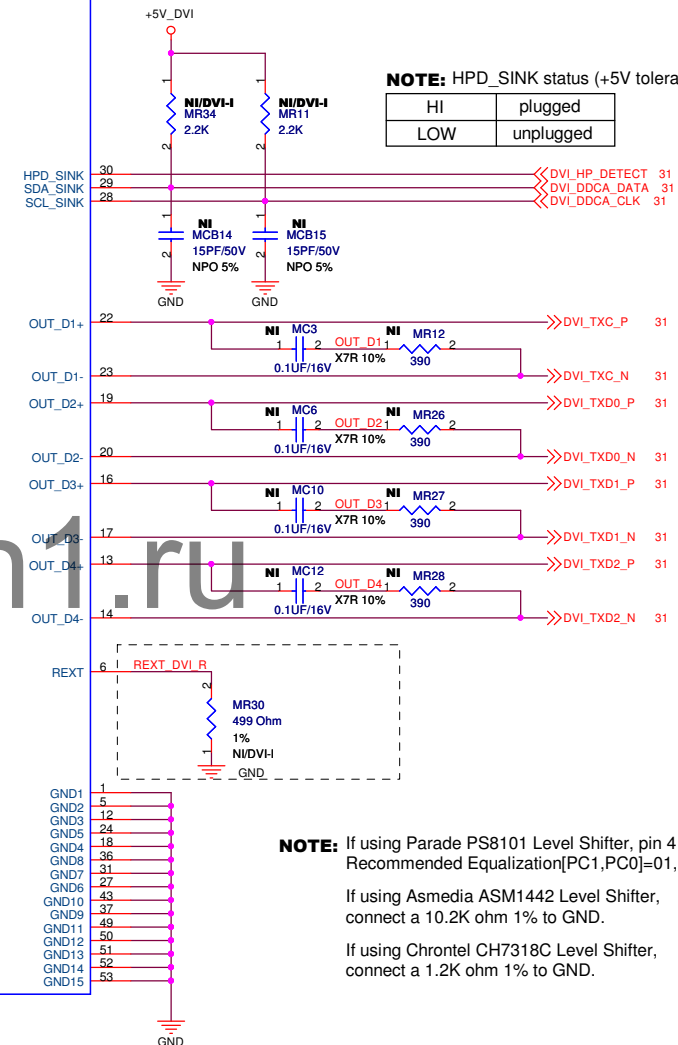
OC_3 (Pin10)	OC_2 (Pin6)	OC_1 (Pin4)	OC_0 (Pin3)	Vswing (mV)	Pre/Deemphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
0	0	1	1	1000	0
0	1	0	0	500	0
0	1	0	1	500	1.5dB
0	1	1	0	500	3.5dB
0	1	1	1	500	6dB
1	0	0	0	400	0
1	0	0	1	400	3.5dB
1	0	1	0	400	6dB
1	0	1	1	400	9dB
1	1	0	0	1000	0
1	1	0	1	1000	-3.5dB
1	1	1	0	1000	-6dB
1	1	1	1	1000	-9dB

NOTE: Pericom PI3VDP411LS

EQ0 (Pin34)	EQ1 (Pin35)	Equalization (dB)
0	0	3
0	1	7.2
1	0	10
1	1	12

NOTE:

OE*	IN_D Termination	OUT_D Outputs
1	Hi-Z	Hi-Z
0	50ohm	Active



PEGATRON DT-MB RESTRICTED SECRET

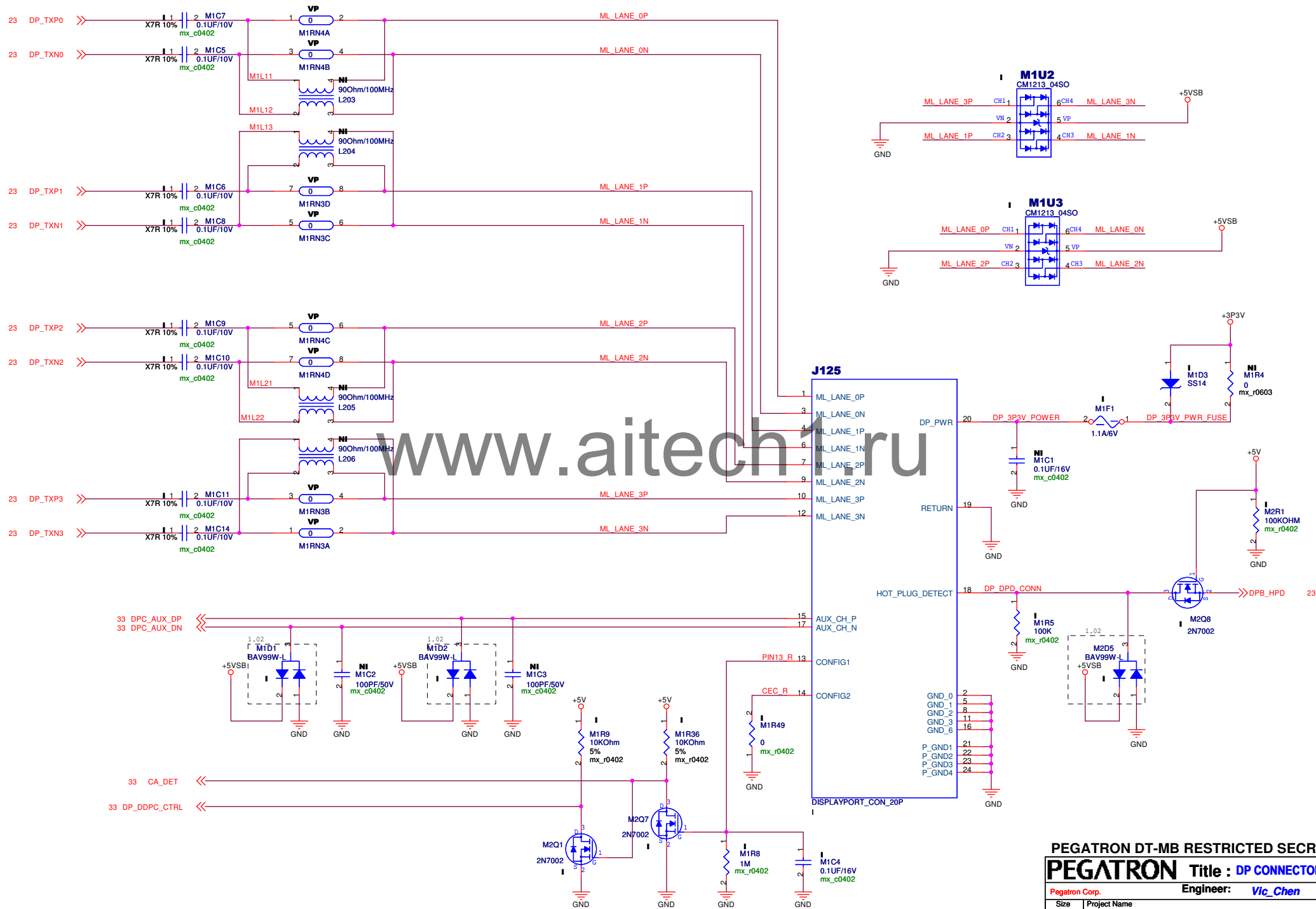
PEGATRON Title : DVI Level shifter

Pegatron Corp. Engineer: Vic\_Chen

Size A3	Project Name IPMIP-DP	Rev 1.01
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Date: Wednesday, April 07, 2010 Sheet 30 of 68





PEGATRON DT-MB RESTRICTED SECRET

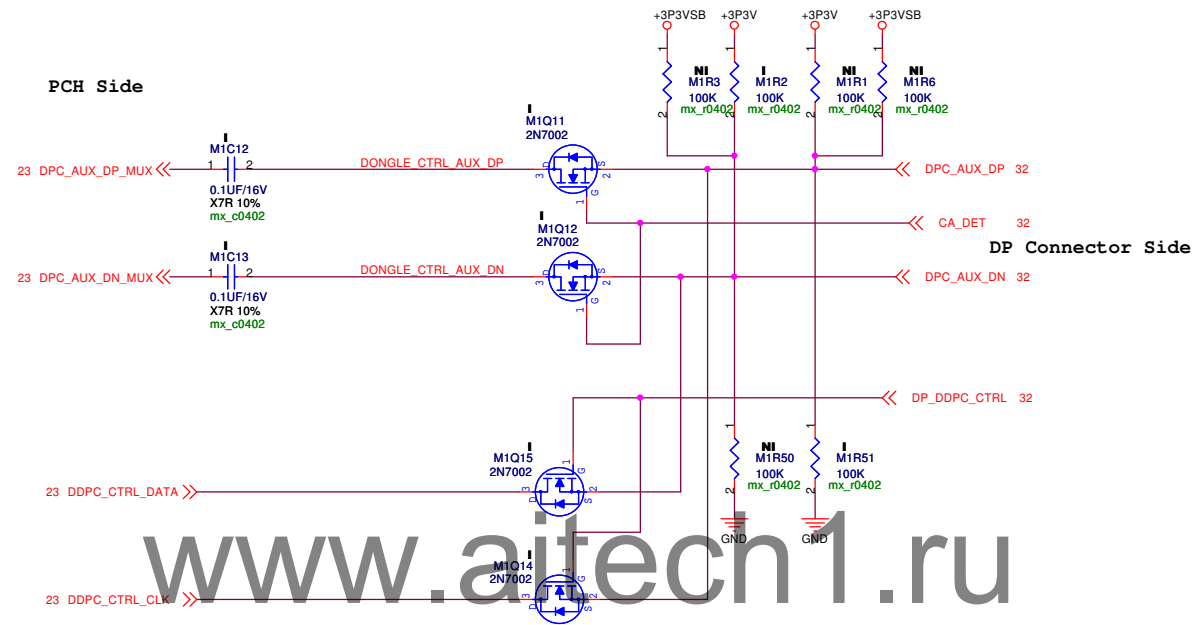
**PEGATRON** Title : DP CONNECTOR

Pegatron Corp. Engineer: Vic Chen

Size A3	Project Name IPMP-DP	Rev 1.01
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Date: Wednesday, April 07, 2010 Sheet 32 of 68

# Display Port to HDMI/DVI Dongle control



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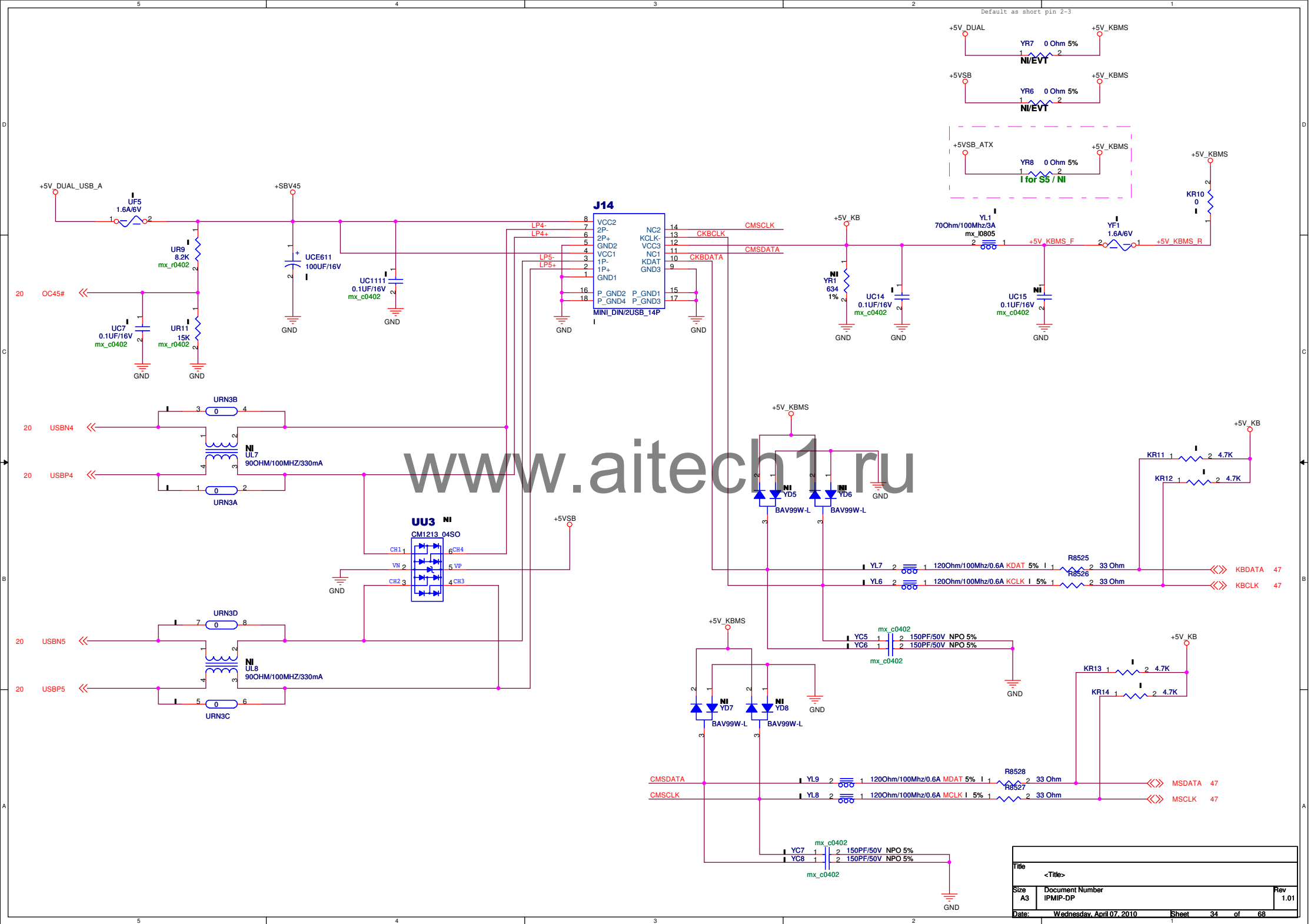
PEGATRON DT-MB RESTRICTED SECRET

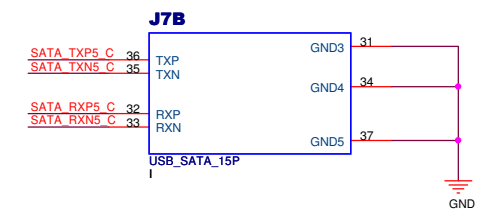
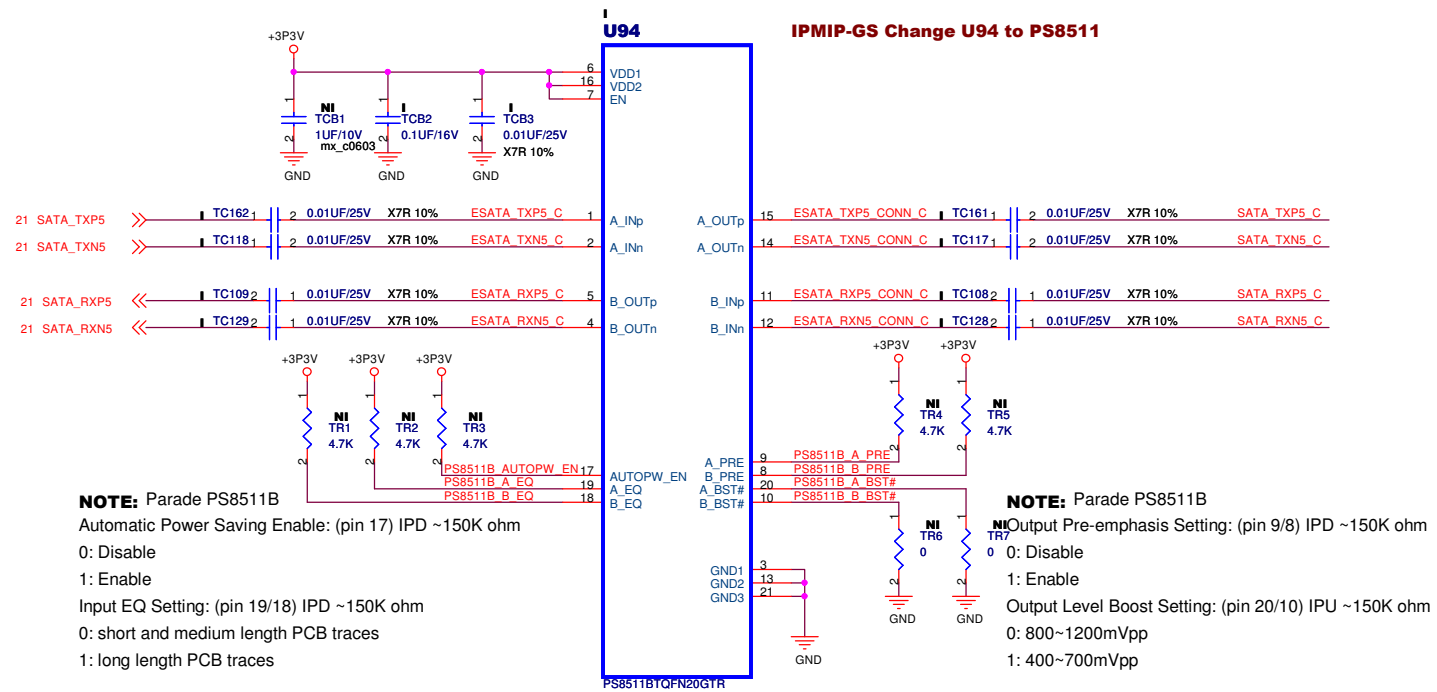
**PEGATRON** Title : DP DONGLE

Pegatron Corp. Engineer: Vic\_Chen

Size A3 Project Name IPMIP-DP Rev 1.01

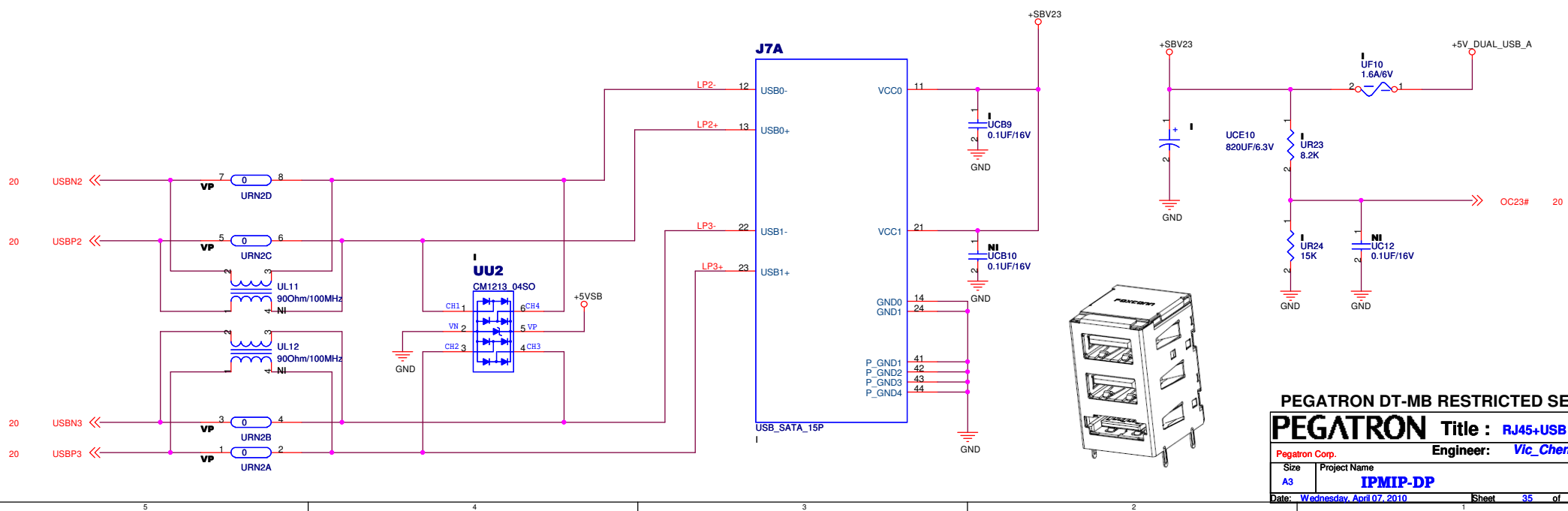
Date: Wednesday, April 07, 2010 Sheet 33 of 68

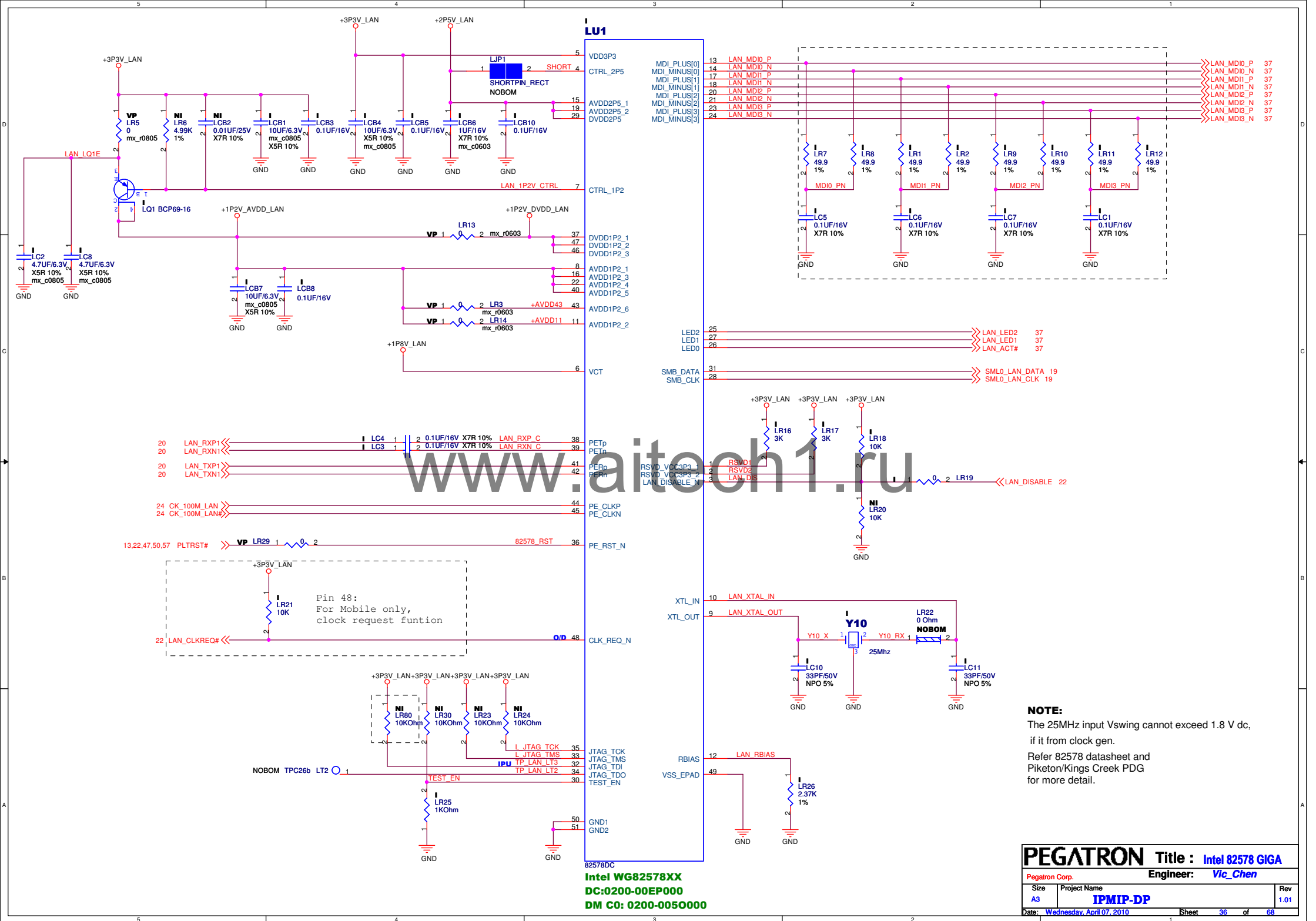




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E-SATA + Dual USB CONNECTOR



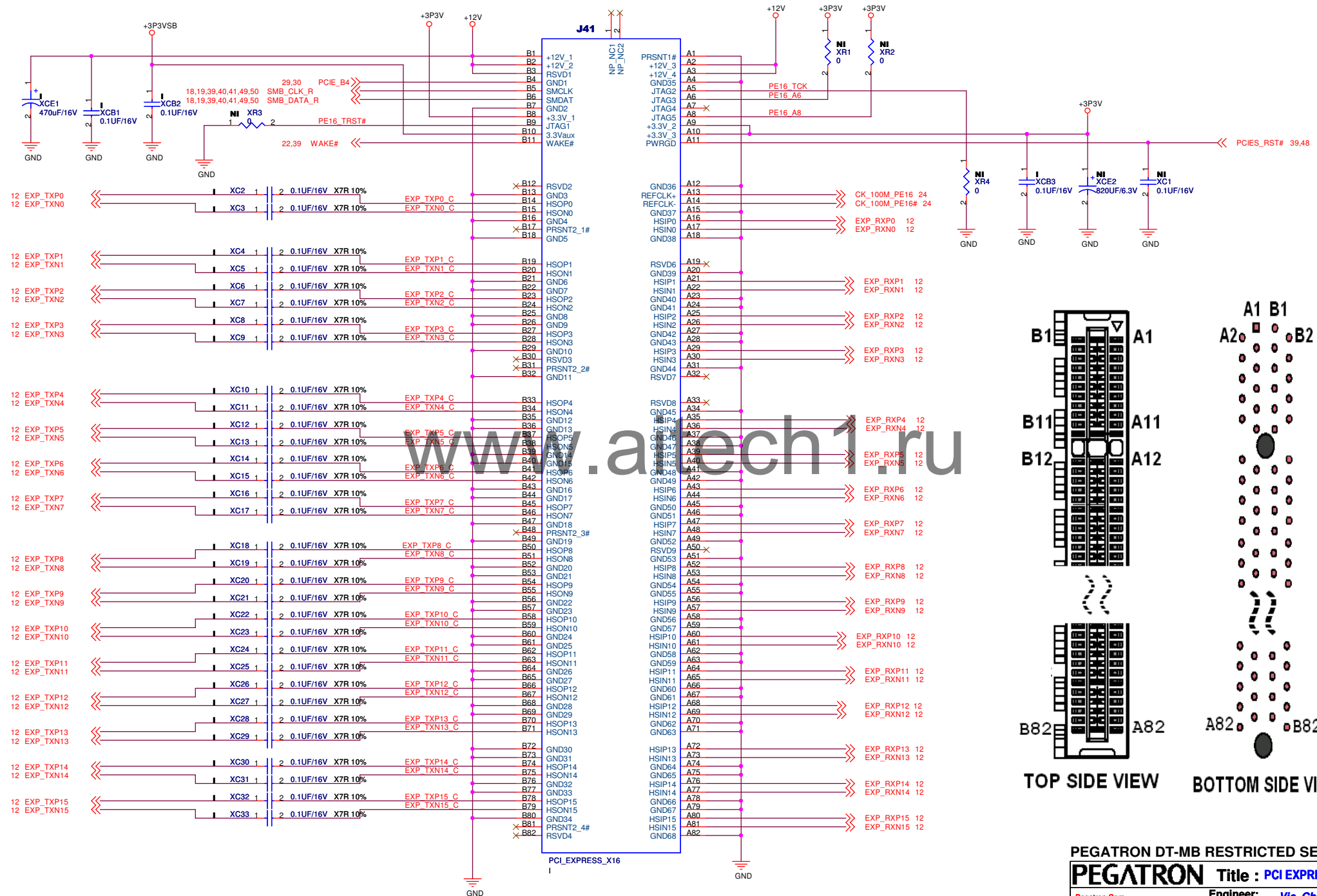


Intel WG82578XX  
DC:0200-00EP000  
DM C0: 0200-0050000





# PCI EXPRESS X16 Graphics Card Slot



TOP SIDE VIEW

BOTTOM SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

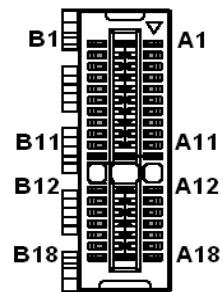
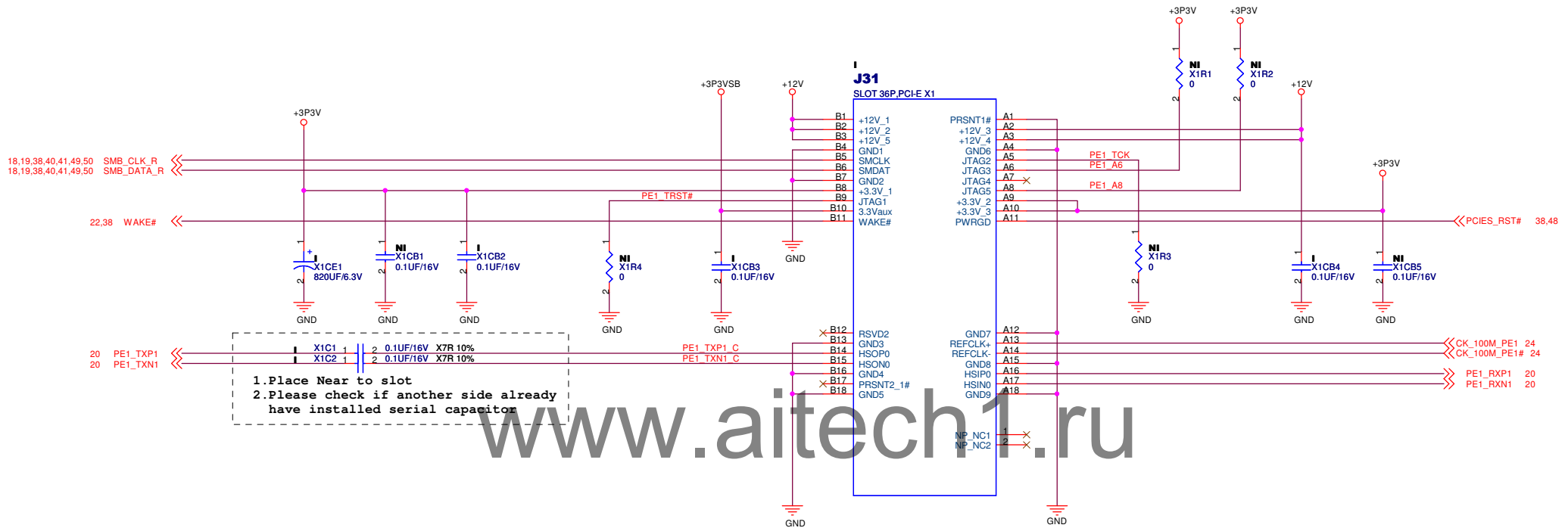
**PEGATRON** Title : PCI EXPRESS X16

Pegatron Corp. Engineer: **Vic Chen**

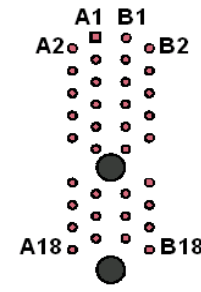
Size A3 Project Name **IPMIP-DP** Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 38 of 68

# PCI Express x1 SLOT



TOP SIDE VIEW



BOTTOM SIDE VIEW

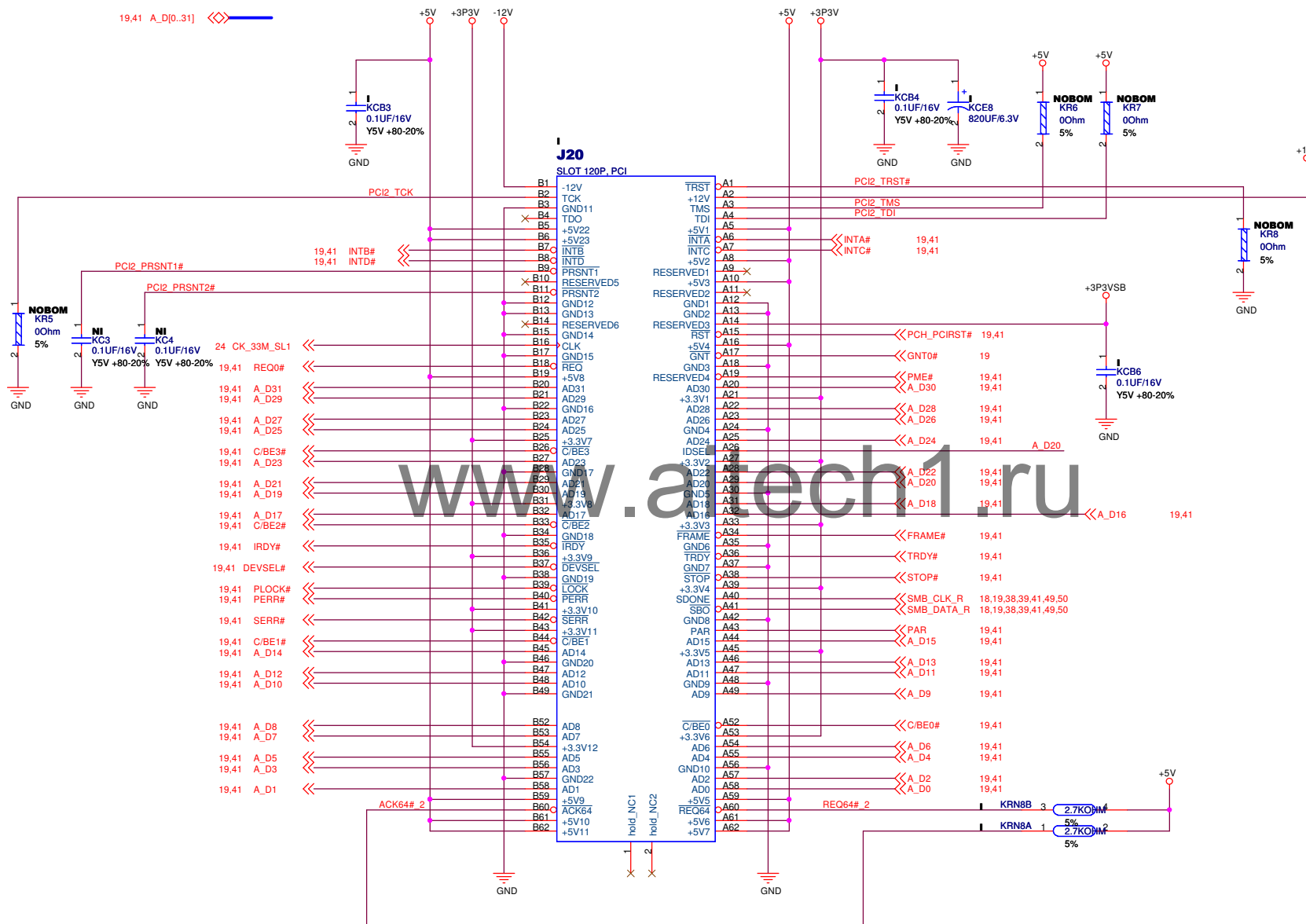
PEGATRON DT-MB RESTRICTED SECRET

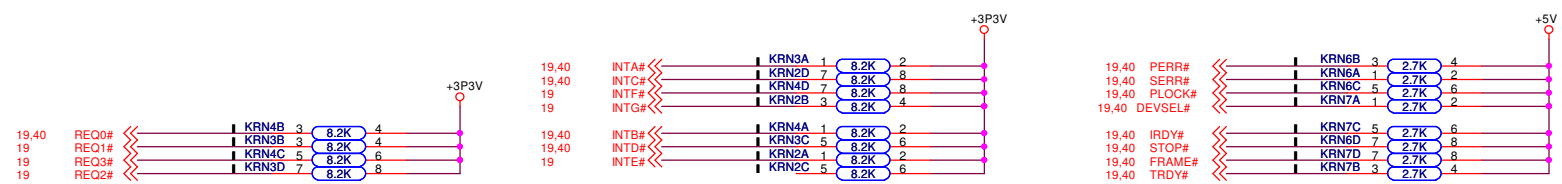
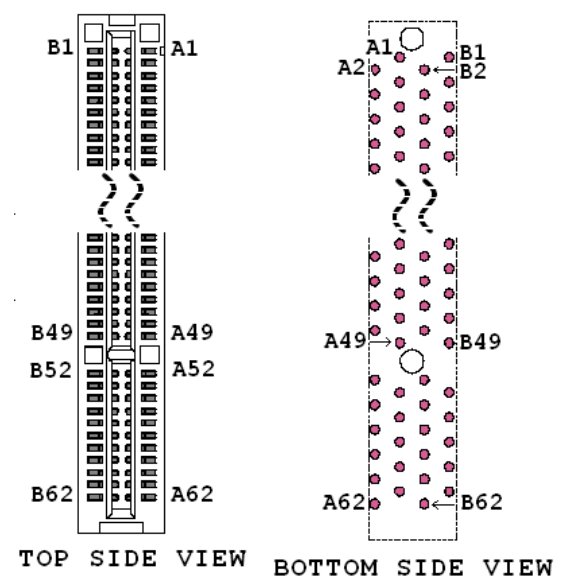
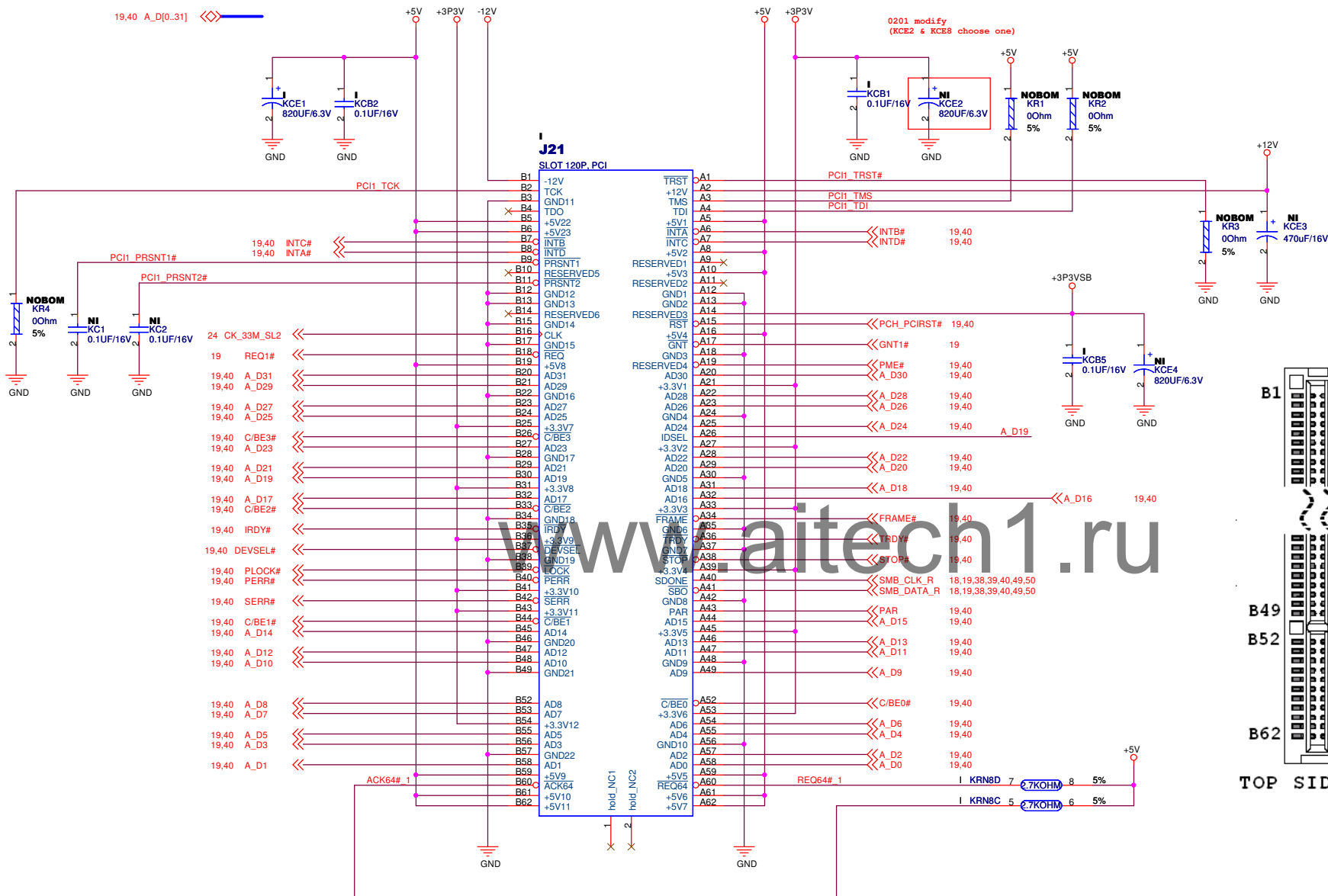
**PEGATRON** Title : **PCI EXPRESS X1**

Pegatron Corp. Engineer: **Vic\_Chen**

Size A3 Project Name **IPMIP-DP** Rev 1.01

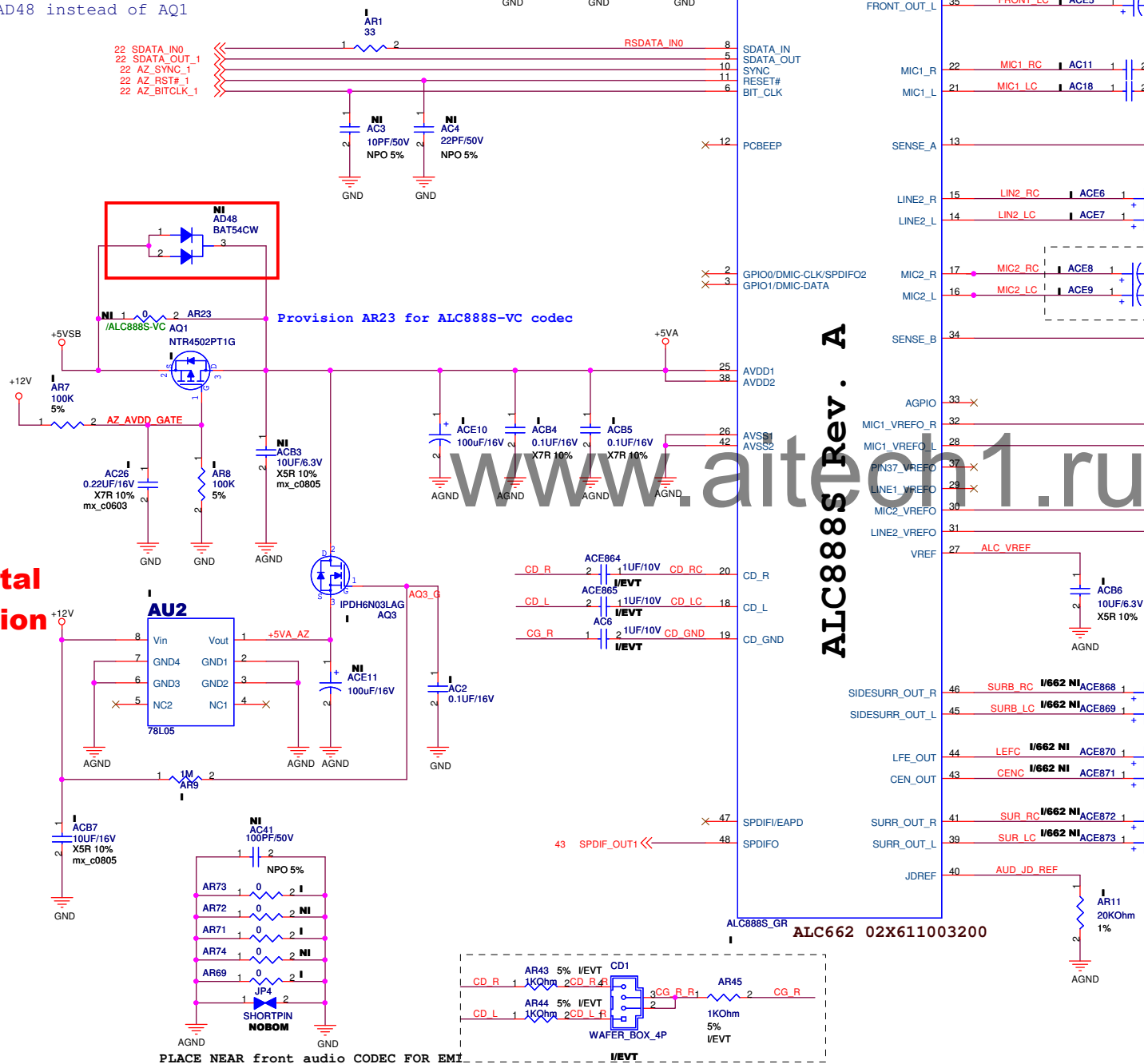
Date: Wednesday, April 07, 2010 Sheet 39 of 68





For some power supply , +5VSB  
drop before +12V when AC  
power out (S0 --> G3) , +12V  
will current back to +5VSB  
If your power supply has this  
sequence issue , please  
install AD48 instead of AQ1

**Please note:**  
**AZ\_BITCLK need add**  
**a serial res(22 ohm)**  
**near SB side**



ALC888\$ Rev. A

**ALC662 02X611003200**

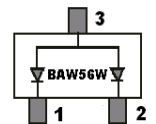
**PEGATRON DT-MB RESTRICTED SECRET**

**PEGATRON** Title : **AUDIO CODEC**

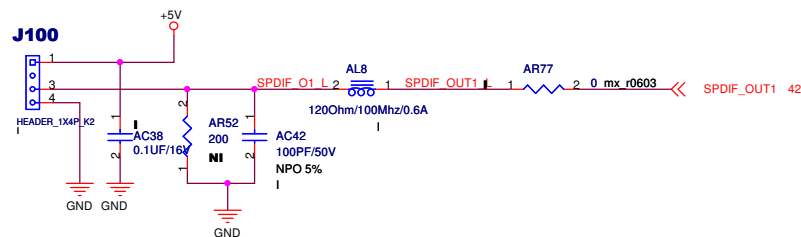
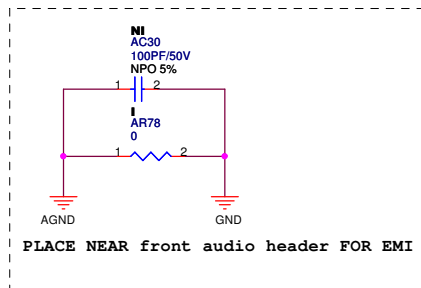
**Engineer:** Vic\_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

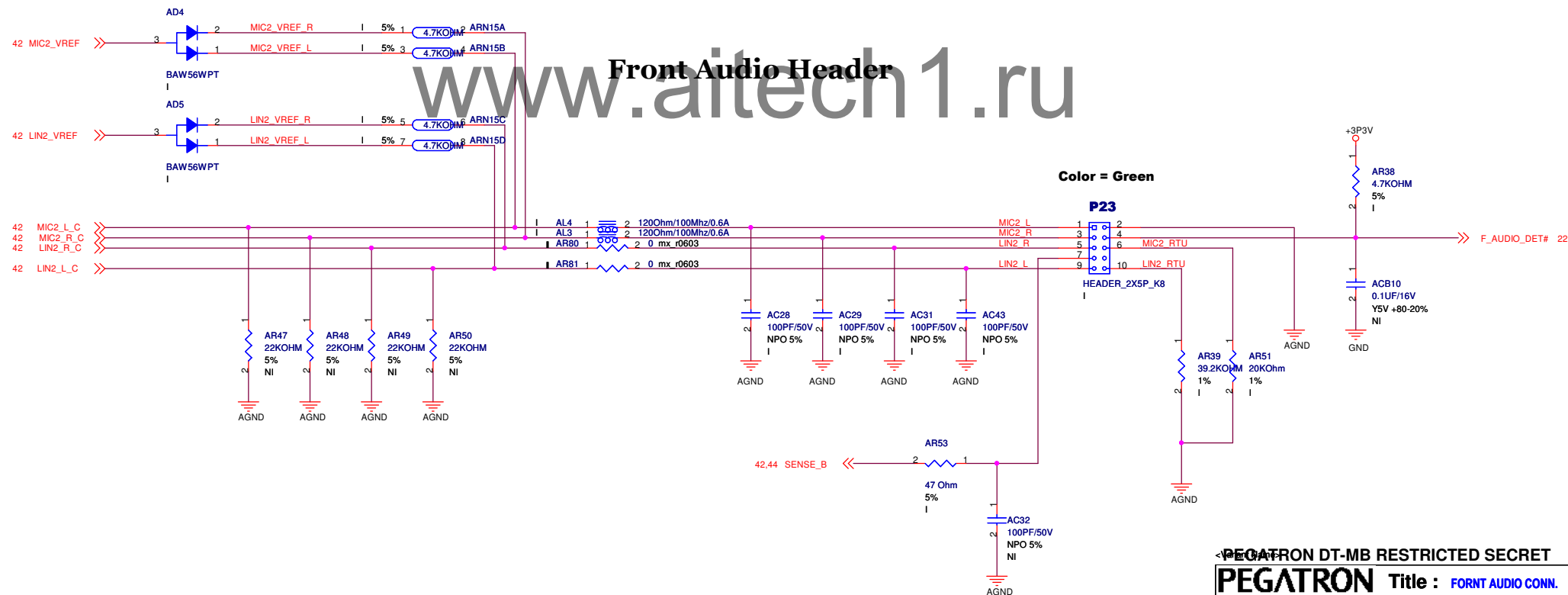
Date: Wednesday, April 07, 2010 Sheet 42 of 68



TOP SIDE VIEW



But for other customers (ex, Intel, EPSON, FSC, Dell.....etc), they might don't need 6+3 configuration, just general 6+2 type. If so, please change LINE1 (Pin 23/24) to Rear Line-In port instead of CD-IN, because CD-IN (Pin 18/19/20) port is only dedicated input port and can't retasking



<PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : FORNT AUDIO CONN.

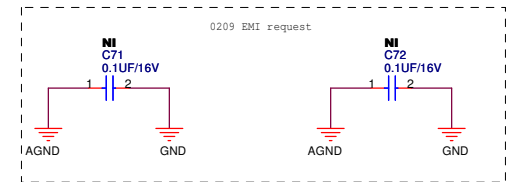
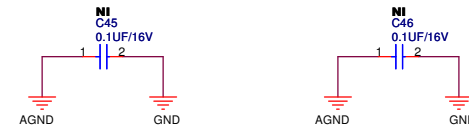
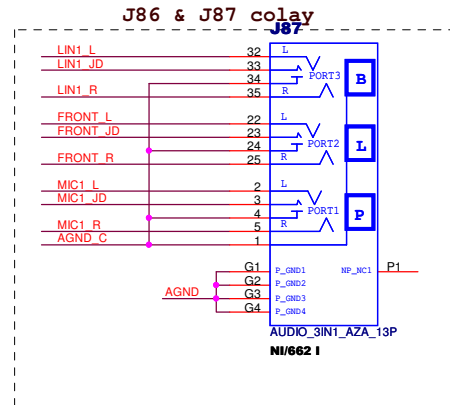
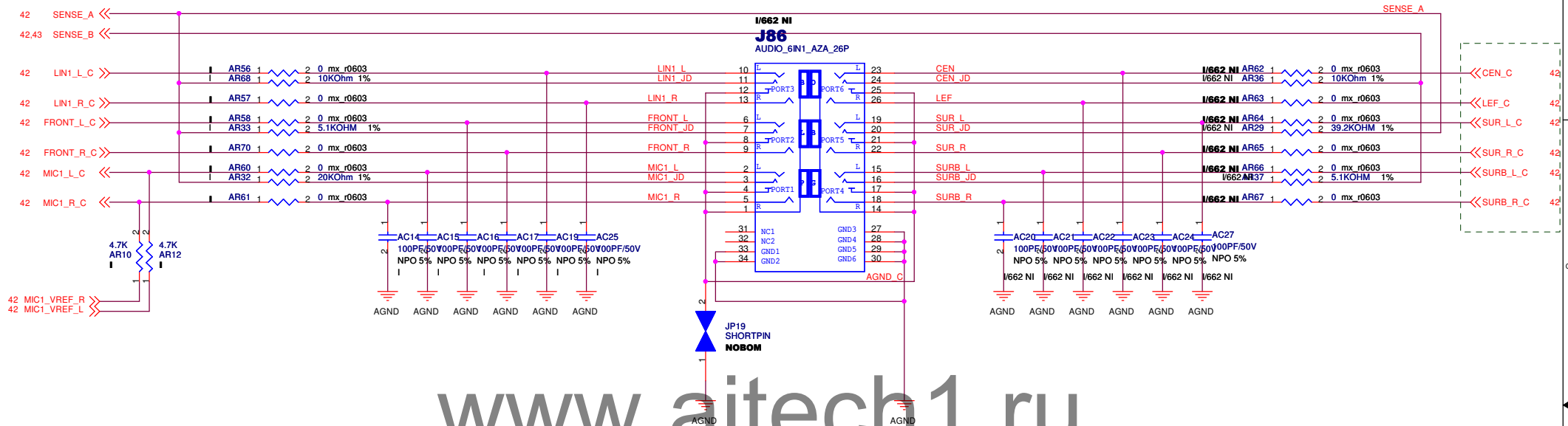
Pegatron Corp. Engineer: Vic Chen

Size A3 Project Name IPMP-DP Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 43 of 68

# Azalia Rear Audio Connector

IPMIP-GS R1.01 Change port



PEGATRON DT-MB RESTRICTED SECRET

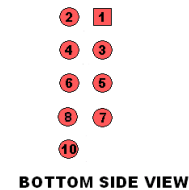
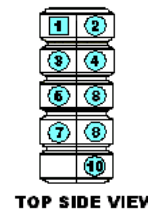
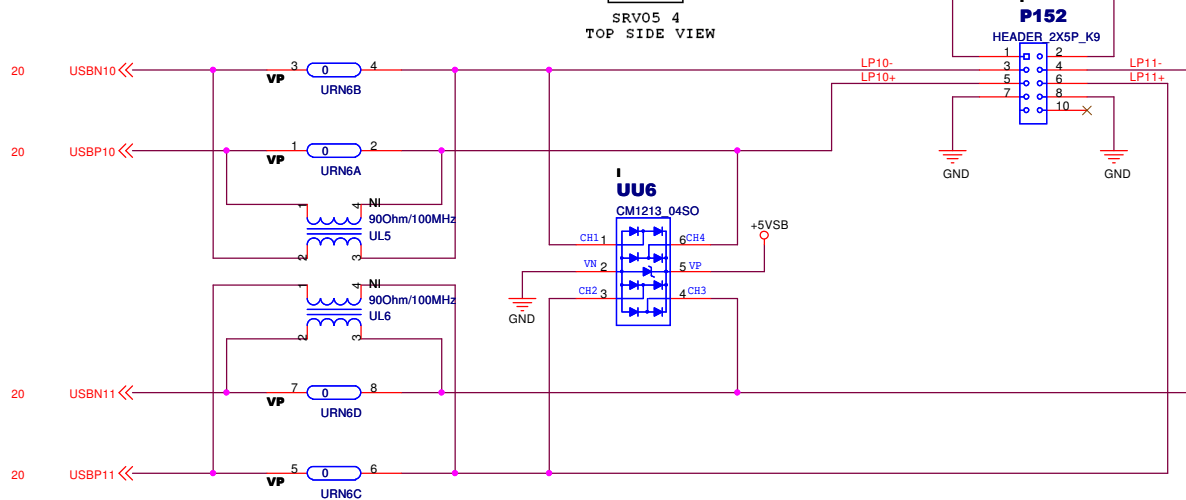
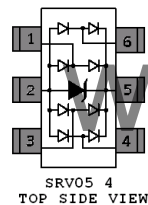
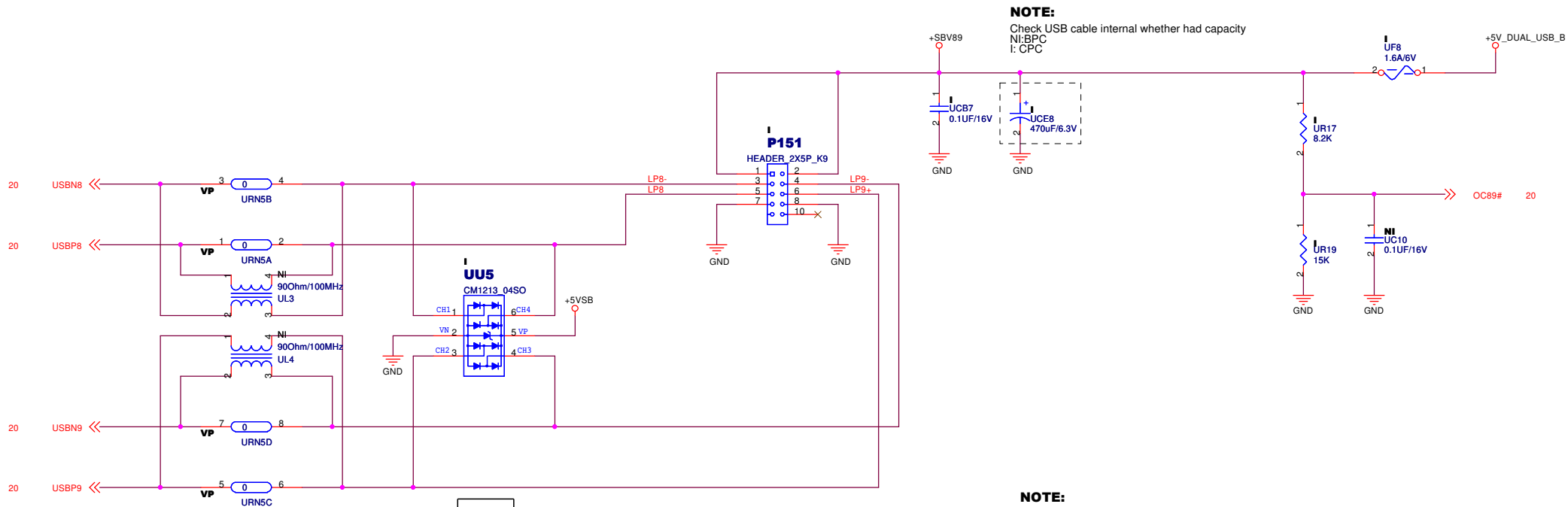
**PEGATRON** Title : REAR AUDIO CONN.

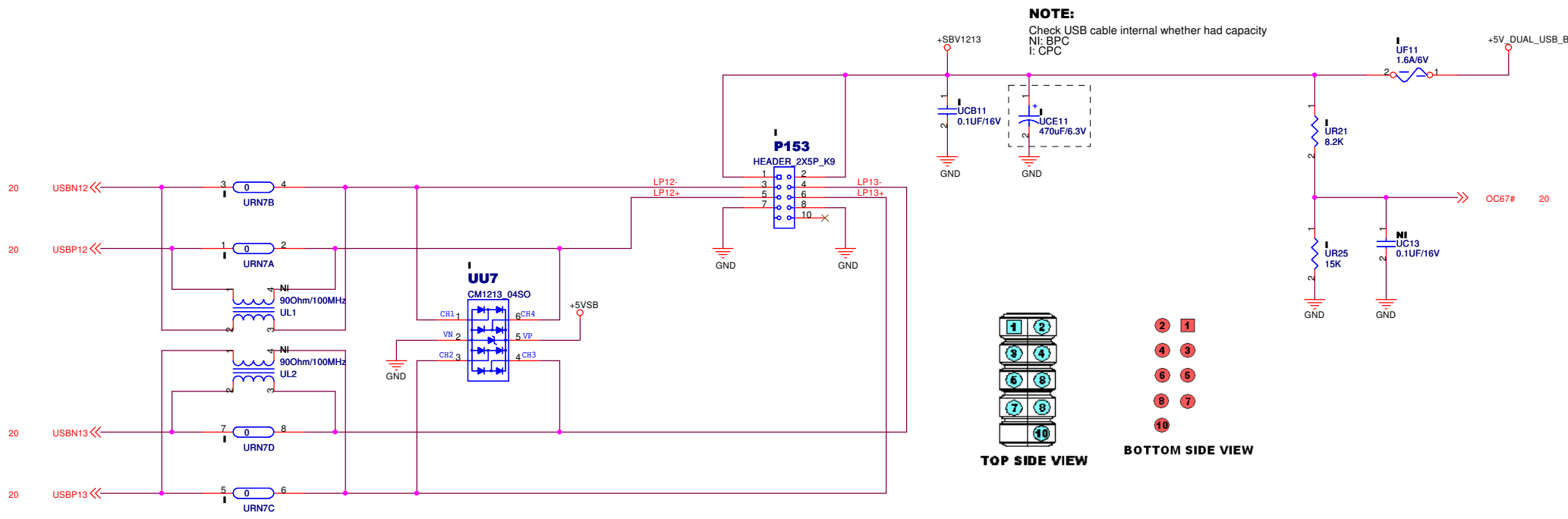
Pegatron Corp. Engineer: Vic\_Chen

Size A3	Project Name IPMIP-DP	Rev 1.01
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Date: Wednesday, April 07, 2010 Sheet 44 of 68

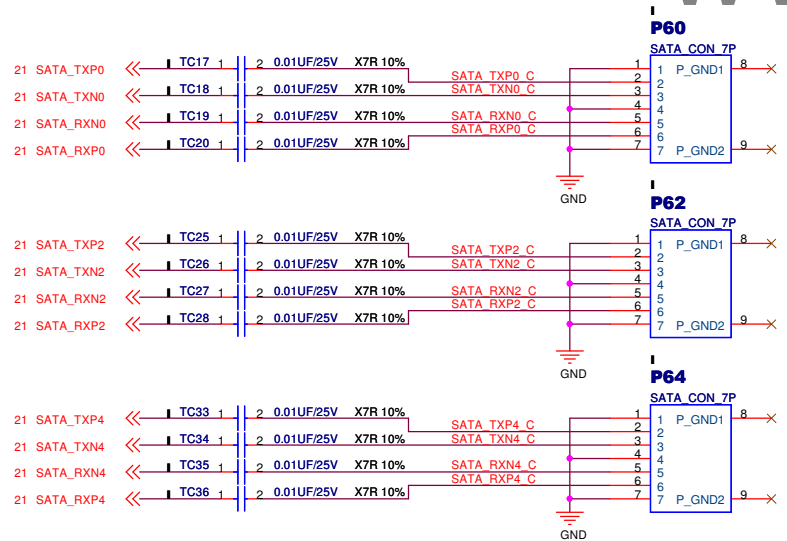






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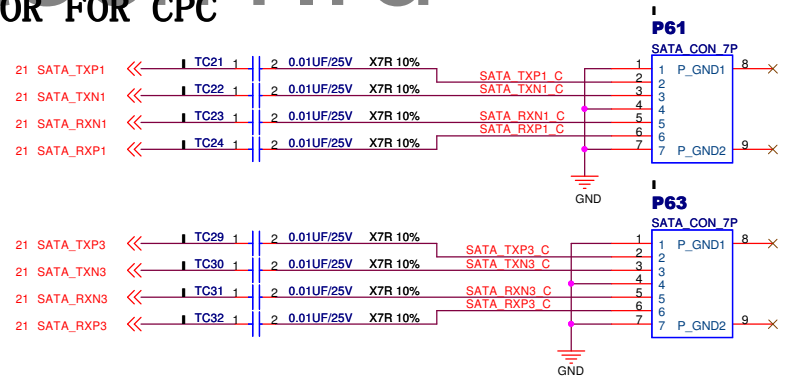
SATA CONNECTOR FOR CPC



**SATA CONTROLLER #1  
(PRIMARY MASTER)  
COLOR = RED**

**SATA CONTROLLER #1  
(PRIMARY MASTER)  
COLOR = RED**

**SATA CONTROLLER #2  
(PRIMARY MASTER)  
COLOR = RED**



**SATA CONTROLLER #1  
(SECONDARY MASTER)  
COLOR = RED**

**SATA CONTROLLER #1  
(SECONDARY MASTER)  
COLOR = RED**

**Pin49:**  
System clock input: 24/48  
MHz

**Pin 39: SERIRQ**  
Please check if SB side already  
have a pull-up resistor!

22.50 LAD0  
22.50 LAD1  
22.50 LAD2  
22.50 LAD3  
22.50 LFRAME#  
22 LDRO0#  
24 CK\_30M\_SIO  
21.50 SERIRQ  
8 CK\_48M\_SIO

34 KBCLK  
34 KBDATA  
34 MSCLK  
34 MSDATA  
21 RST\_KB#  
21 A20GATE

56 DCD1#  
56 RI1#  
56 CTS1#  
56 DTR1#  
56 RTS1#  
56 DSR1#  
56 TXD1  
56 RXD1

55 XSTB#  
55 XAFD#  
55 ERROR#  
55 ACK#  
55 BUSY  
55 PE  
55 SLCT  
55 XPD0  
55 XPD1  
55 XPD2  
55 XPD3  
55 XPD4  
55 XPD5  
55 XPD6  
55 XPD7  
55 XSLIN#  
55 XINIT#

108 SMBD\_M/STB#/GP87  
107 SMBD\_R/AFD#/GP86  
106 ERR#  
103 ACK#/GP83  
102 BUSY/GP82  
101 PE/GP81  
100 SLCT/GP80  
109 PD0/GP70  
110 PD1/GP71  
111 BUSSIO/PD2/GP72  
112 BUSSIO1/PD3/GP73  
113 BUSSIO2/PD4/GP74  
114 BUSSIO0/PD5/GP75  
115 BUSSIO1/PD6/GP76  
116 BUSSIO2/PD7/GP77  
104 SMBD\_R/SLIN#/GP84  
105 SMBD\_M/INIT#/GP85

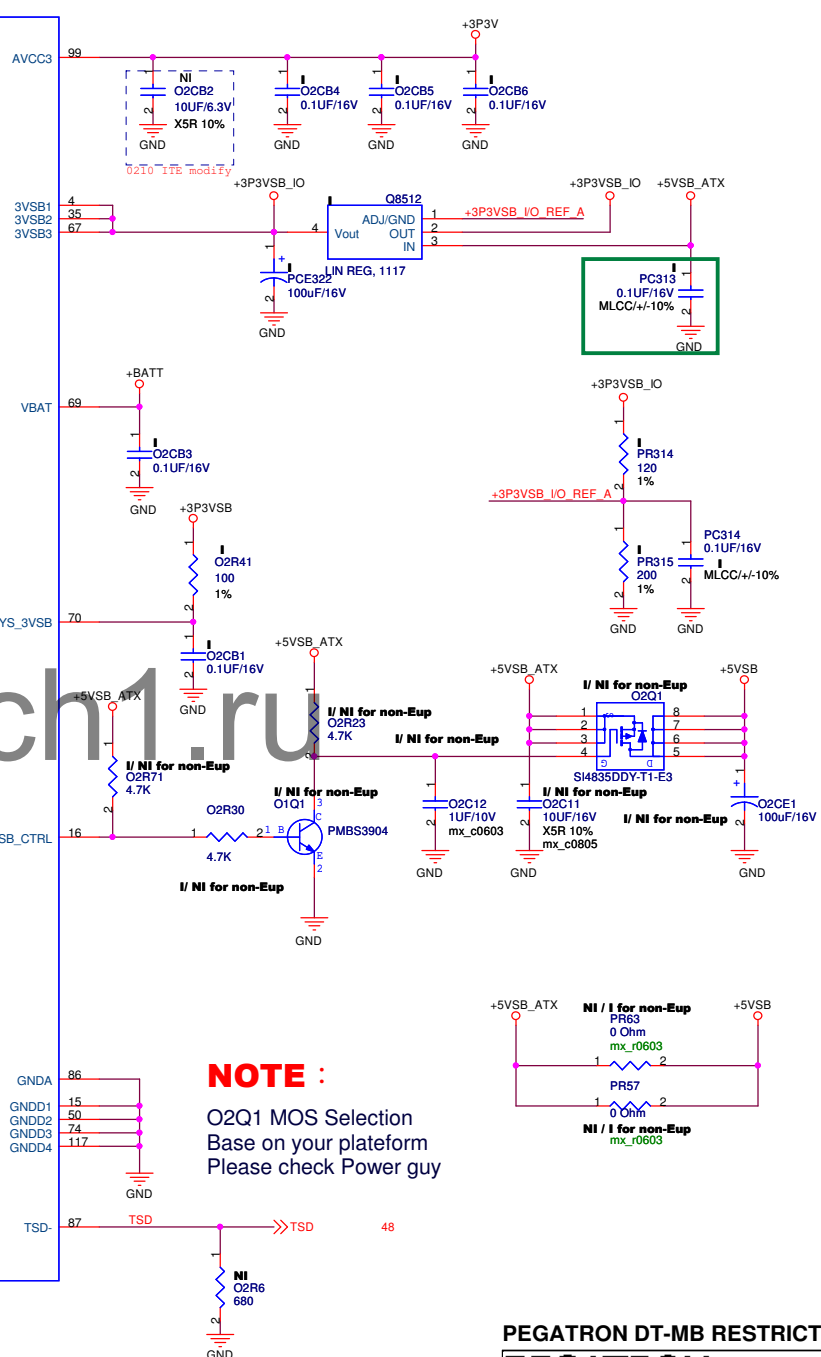
41 LAD0  
42 LAD1  
43 LAD2  
44 LAD3  
40 LFRAME#  
38 LDRO0#  
37 LFRAME#  
47 LFRAME#  
39 SERIRQ  
49 CKIN

80 KDAT/GP61  
81 KCLK/GP60  
82 MDAT/GP57  
83 MCLK/GP56  
45 KRST#/GP62  
46 GA20/JP5

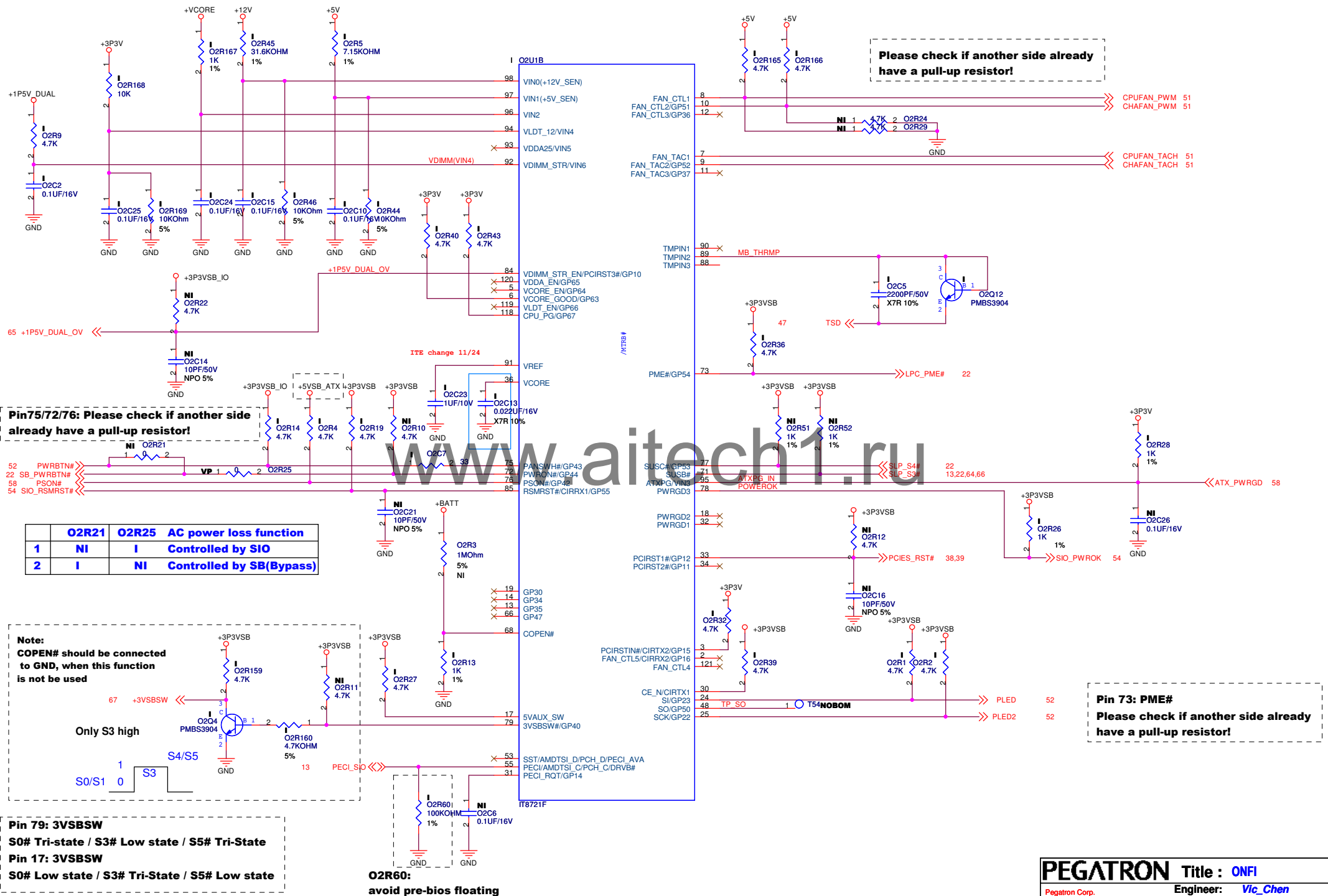
127 DCD1#  
128 RI1#  
126 CTS1#  
122 DTR1#/JP4  
123 RTS1#  
124 DSR1#  
125 SOUT1/JP3  
SIN1

26 DCD2#  
28 RI2#  
27 CTS2#  
29 DTR2#  
23 FAN\_TACS/RTS2#/GP24  
22 FAN\_TACA/DSR2#/GP25  
21 SOUT2/GP26  
20 SIN2/GP27

IT8721F



**NOTE :**  
O2Q1 MOS Selection  
Base on your platform  
Please check Power guy



# SM BUS Control

To PCH, PCI, and PCIE Slot

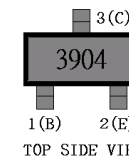
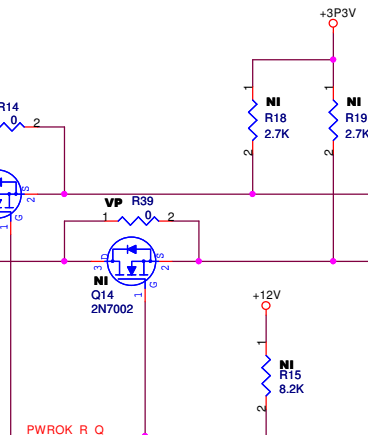
18,19,38,39,40,41,50 SMB\_DATA\_R

18,19,38,39,40,41,50 SMB\_CLK\_R

To Clock Gen, DIMMs, and ITP Debug Port

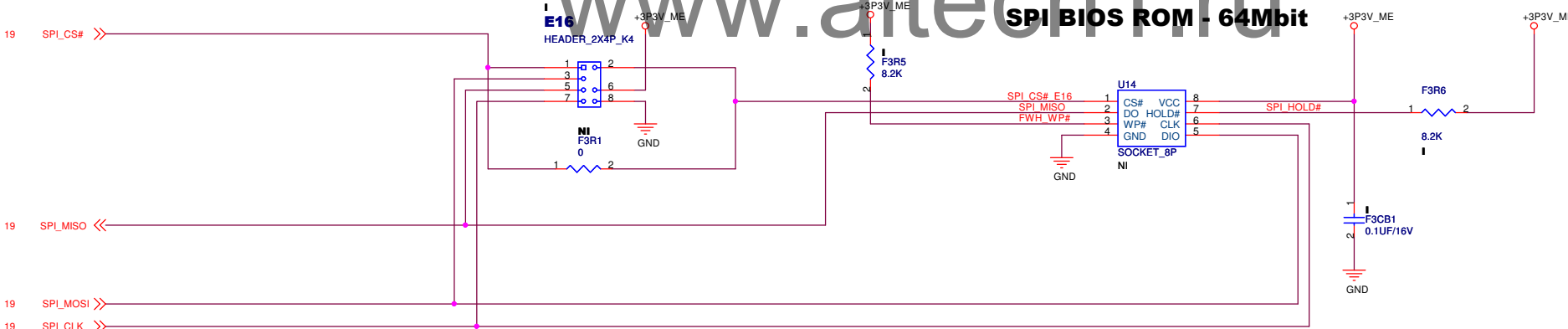
SMB\_DATA\_M 8,16,17,57

SMB\_CLK\_M 8,16,17,57

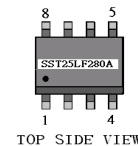
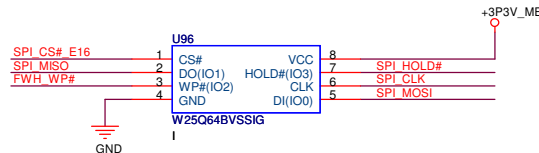


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SPI BIOS ROM - 64Mbit



**IPMIP-GS Change SPI to 64Mb**  
**64Mb: 05X00Z2GE330**  
**32Mb: 05X00Z2FC330**  
**16Mb: 05X00Z2EA330**



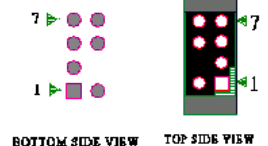
PEGATRON DT-MB RESTRICTED SECRET

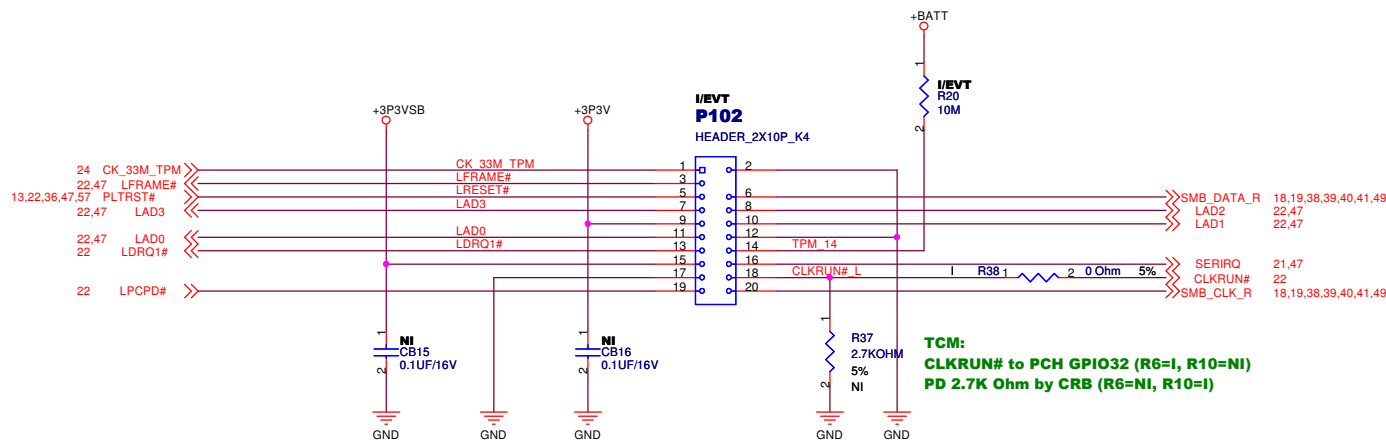
**PEGATRON** Title : SPI FLASH - 8M

Pegatron Corp. Engineer: Vic\_Chen

Size A3 Project Name IPMIP-DP Rev 1.01

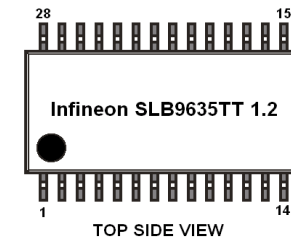
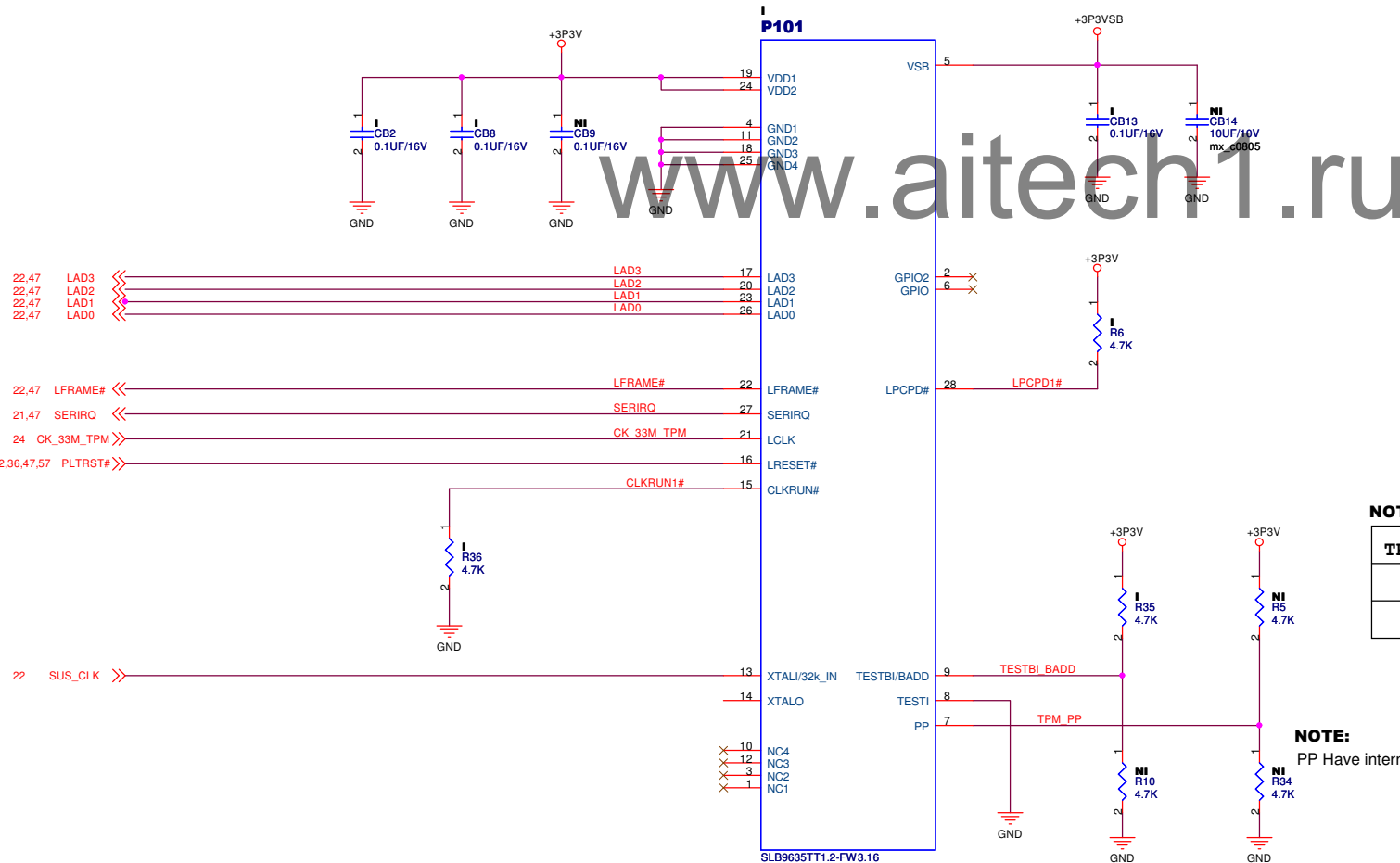
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**BOTTOM SIDE VIEW**

**TOP SIDE VIEW**



**NOTE:**

TPM_BASE_ADDR	I/O SPACE
0	2E
1	4E

**NOTE:**

PP Have internal PULL-DOWN

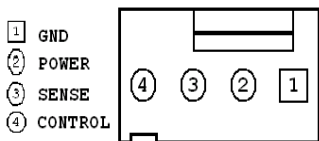
**PEGATRON DT-MB RESTRICTED SECRET**

**PEGATRON** Title : **SATA2 & TPM/TCM**

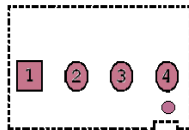
Pegatron Corp. Engineer: **Vic\_Chen**

Size A3 Project Name **IPMIP-DP** Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 50 of 68



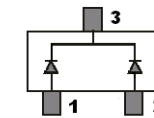
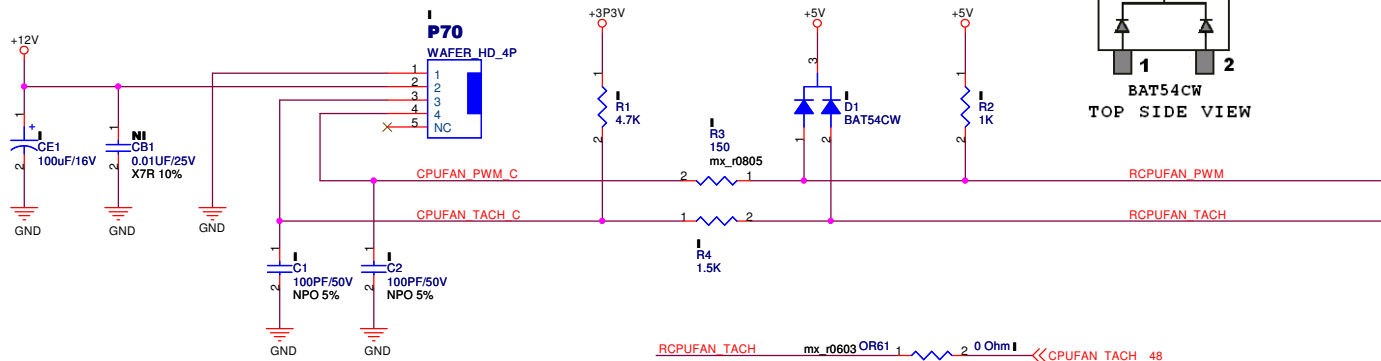
TOP SIDE VIEW



BOTTOM SIDE VIEW

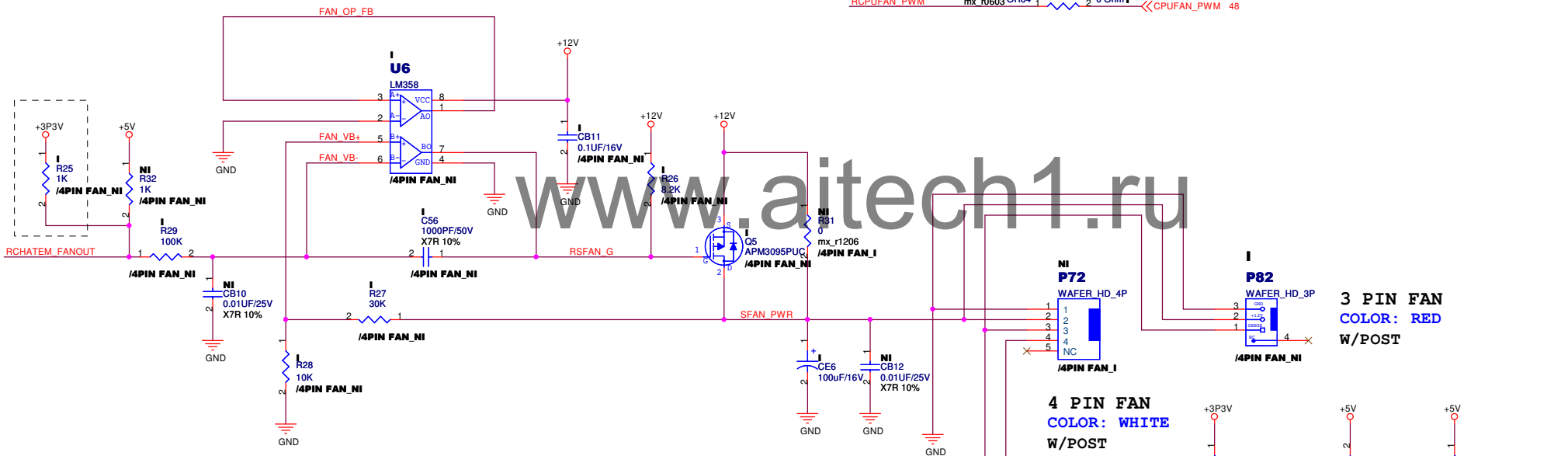
CPU FAN  
COLOR: WHITE  
W/POST

P70  
WAFER\_HD\_4P

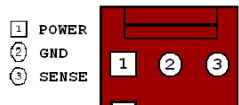


TOP SIDE VIEW

3 & 4 PIN CO-LAYOUT Circuit ( Default 3 pin fan )



BOTTOM SIDE VIEW



TOP SIDE VIEW

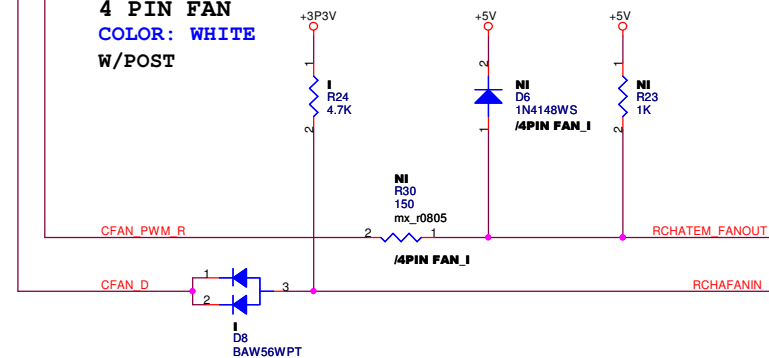
3 PIN FAN  
COLOR: RED  
W/POST

3 PIN FAN  
COLOR: RED  
W/POST

P72  
WAFER\_HD\_4P

4 PIN FAN  
COLOR: WHITE  
W/POST

P82  
WAFER\_HD\_3P

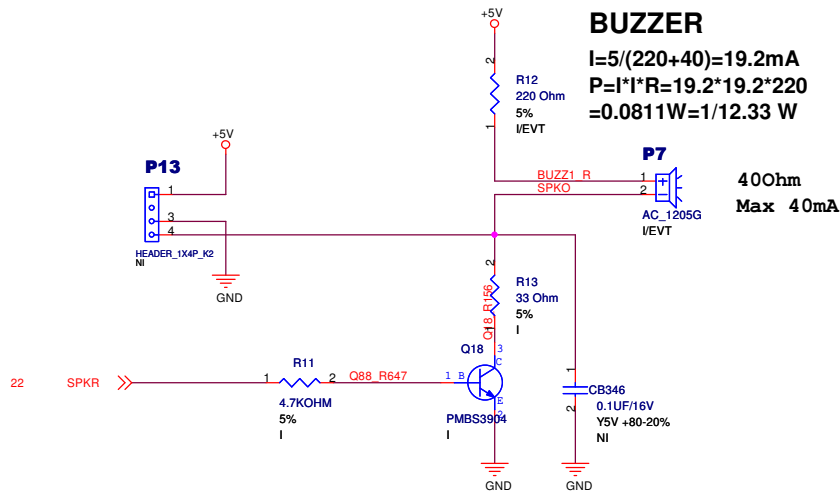
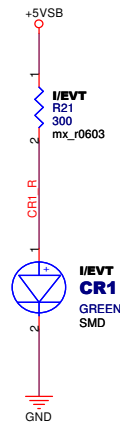


PEGATRON DT-MB RESTRICTED SECRET

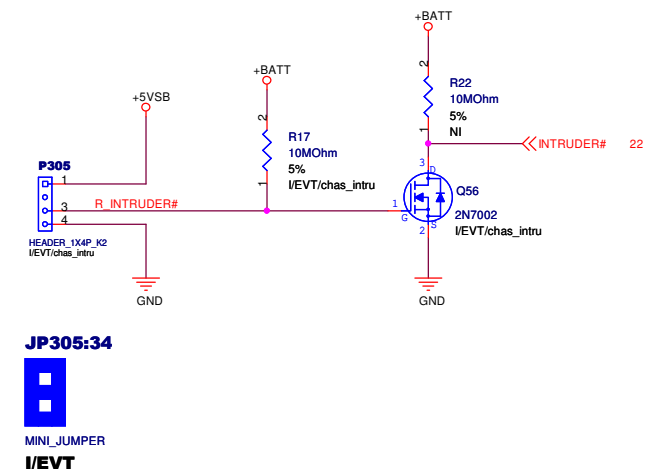
PEGATRON Title : 4-PIN FAN CONN

Pegatron Corp.		Engineer: Vic_Chen	
Size A3	Project Name	IPMIP-DP	Rev 1.01
Date: Thursday, April 08, 2010	Sheet 51	of 68	

+5VSB : GREEN

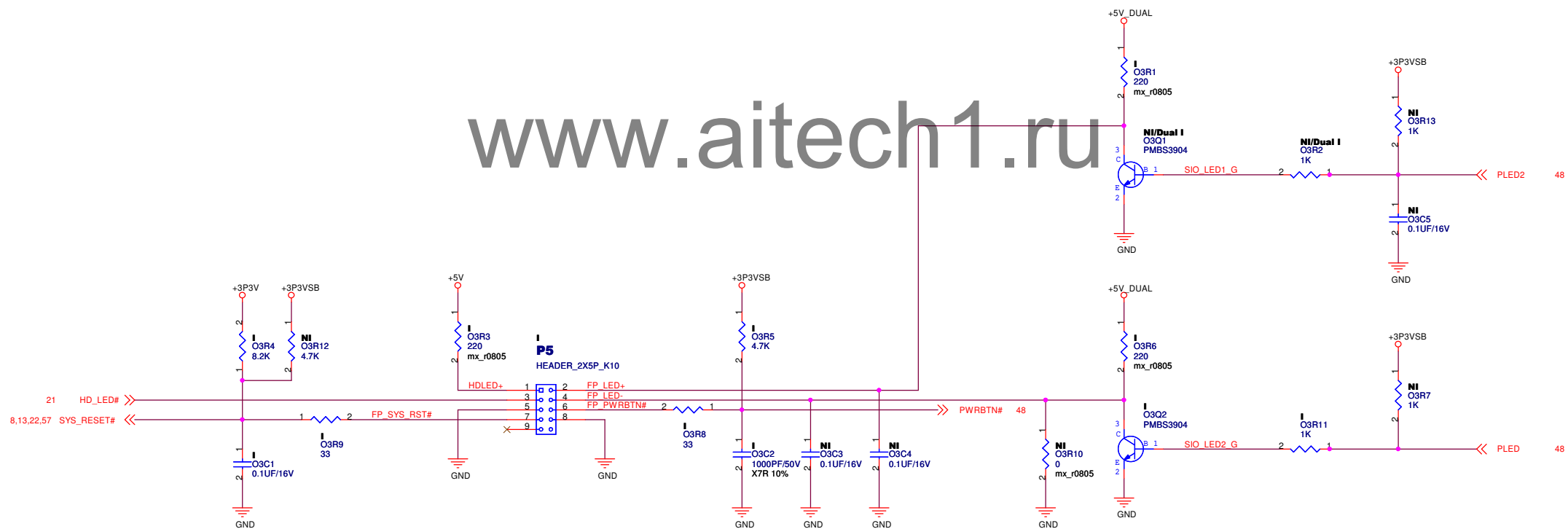


INTRUDER

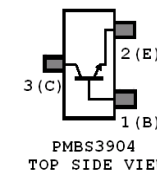


## HPD CONTROL PANEL / LED CIRCUITRY

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FRONT POWER LED COLOR SUPPORT	O3Q1	O3R2			
SINGLE COLOR	NI	NI			
DUAL COLOR	I	I			



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title: FRONT PANEL

Pegatron Corp. Engineer: Vic Chen

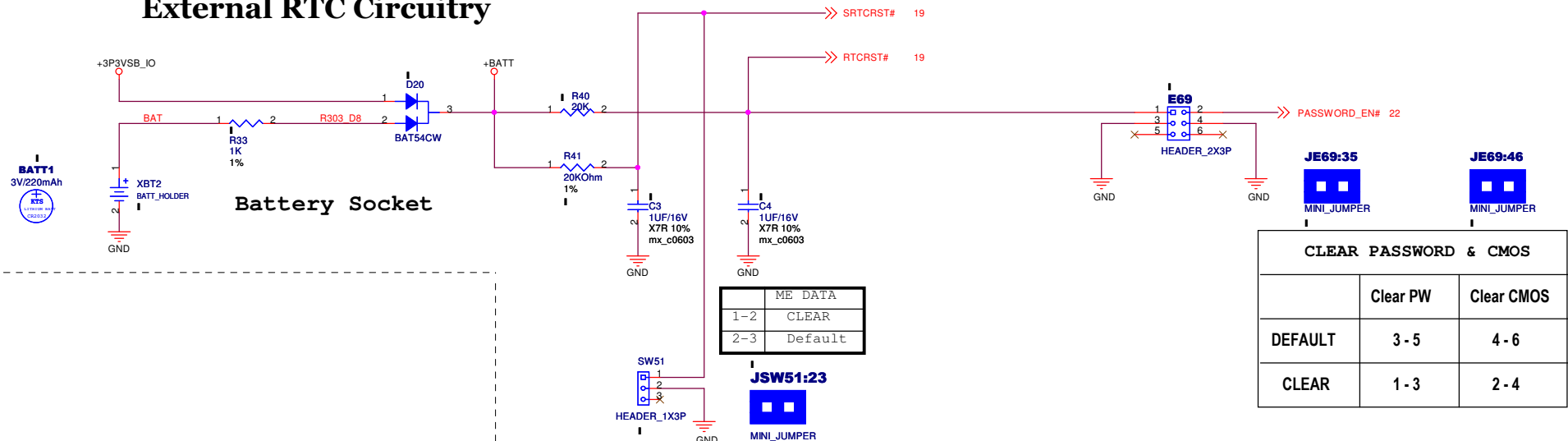
Size A3	Project Name IPMP-DP	Rev 1.01
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Date: Wednesday, April 07, 2010 Sheet 52 of 68

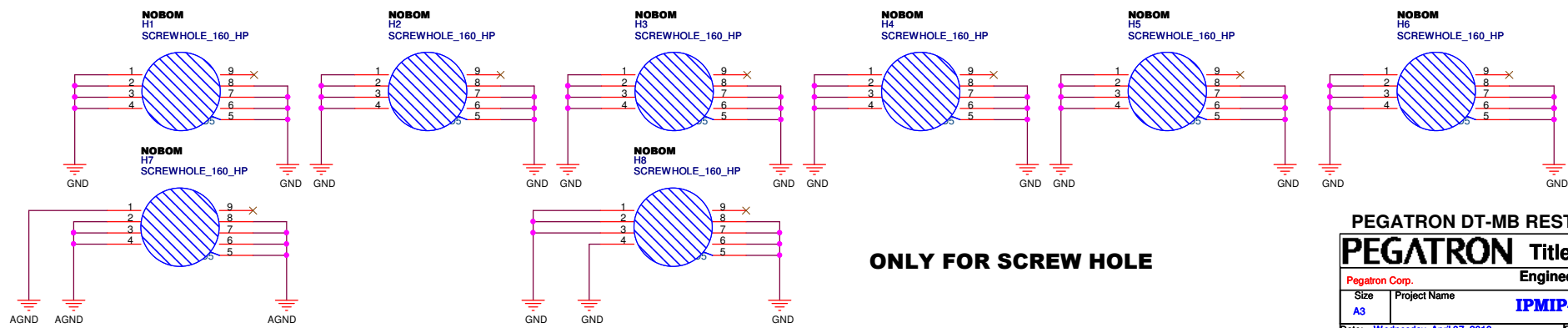


## External RTC Circuitry

## CLEAR CMOS & PASSWORD



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PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : RTC / CMOS / KBMS

Pegatron Corp. Engineer: Vic\_Chen

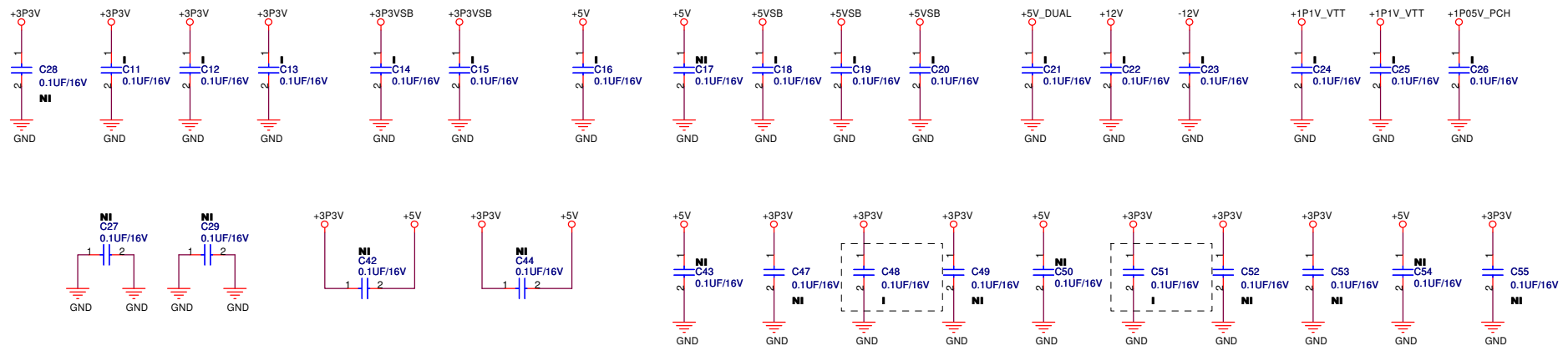
Size A3 Project Name IPMIP-DP Rev 1.01

Date: Wednesday, April 07, 2010 Sheet 53 of 68

# RSMRST CIRCUIT



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PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : RSMRST CIRCUIT

Pegatron Corp. Engineer: Vic Chen

Size A3 Project Name IPMP-DP Rev 1.01

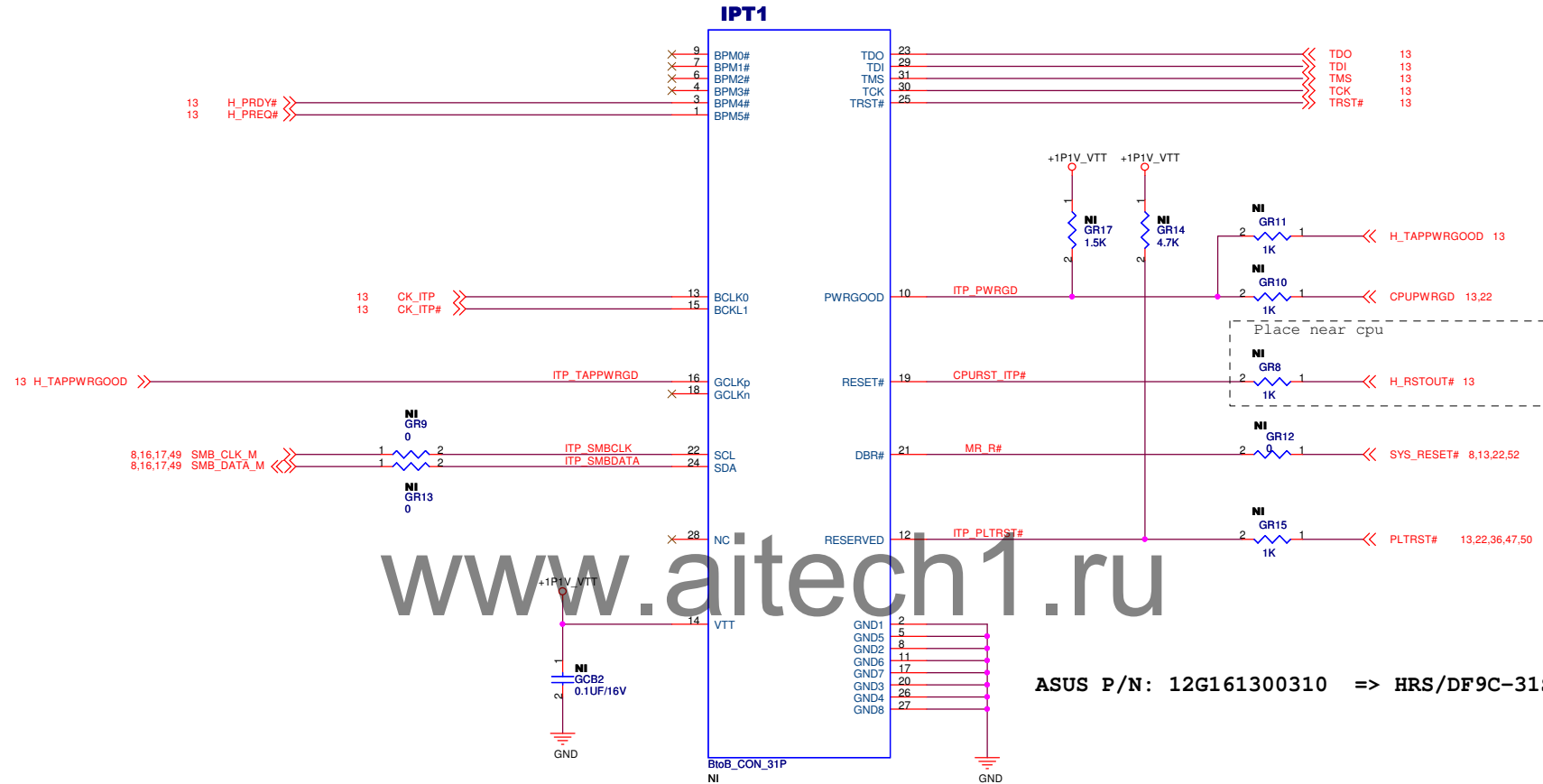
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A diagram of a 32-pin Dual In-Line Package (DIP) component. The package is shown from a top-down perspective, with pins extending from both long sides. The pins are numbered 1 through 32. On the right side, pin 1 is at the top and pin 31 is at the bottom. On the left side, pin 2 is at the top and pin 30 is at the bottom. The package has a central notch and two mounting tabs at the ends.

**HRS/DF9C-31S-1V(22)**  
**TOP SIDE VIEW**

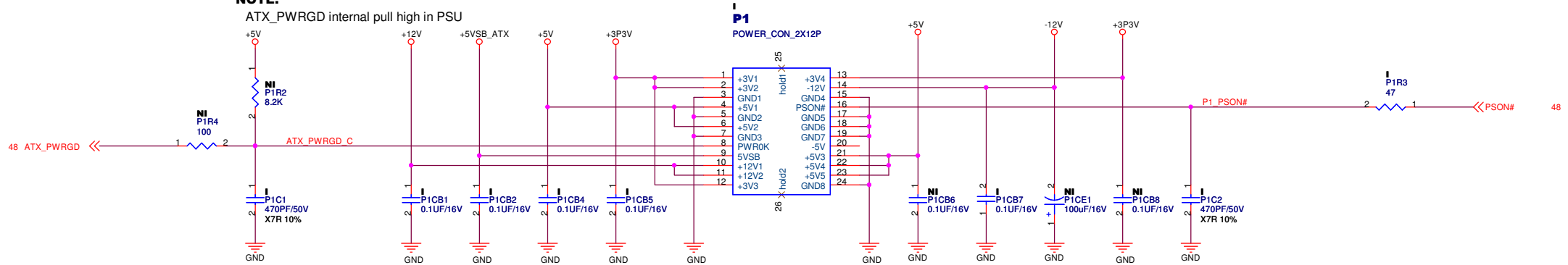


ASUS P/N: 12G161300310 => HRS/DF9C-31S-1V(22)

## ATX POWER\_24P SUPPLY CONNECTOR

### NOTE:

ATX\_PWRGD internal pull high in PSU



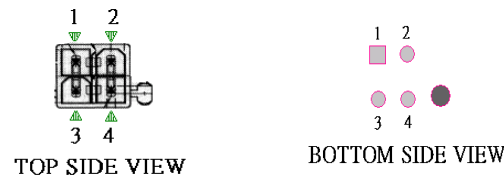
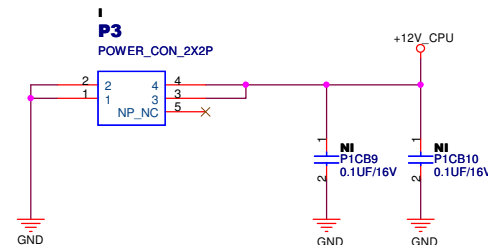
## All of the Caps Around the ATX Power Connector



## PCB

PCB38  
IPMIP-GS R1.00 RED  
08M1-0UX0200

## VRM POWER\_4P SUPPLY CONNECTOR



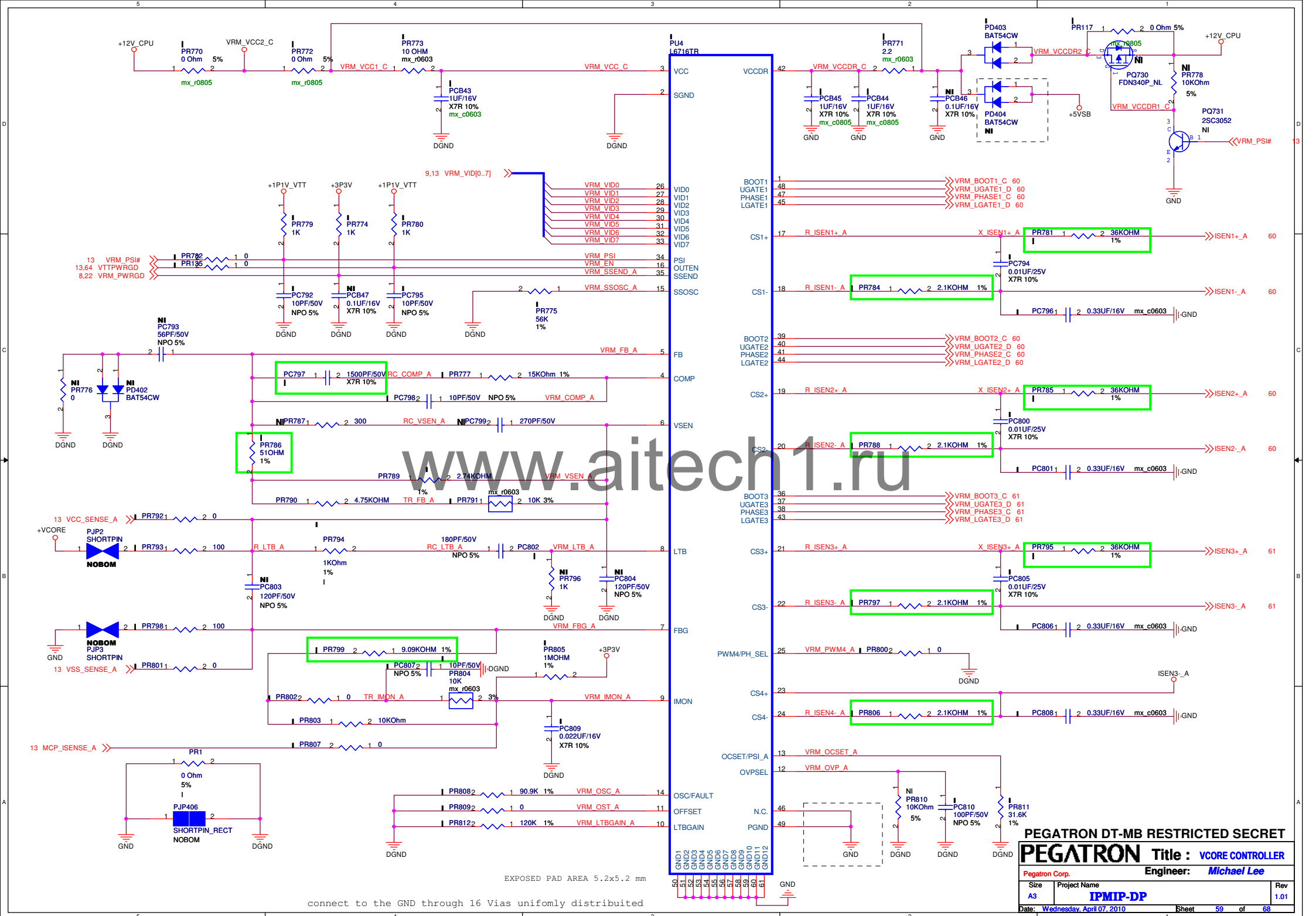
PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : **ATX POWER**

Pegatron Corp. Engineer: **Vic\_Chen**

Size A3 Project Name **IPMIP-DP** Rev 1.01

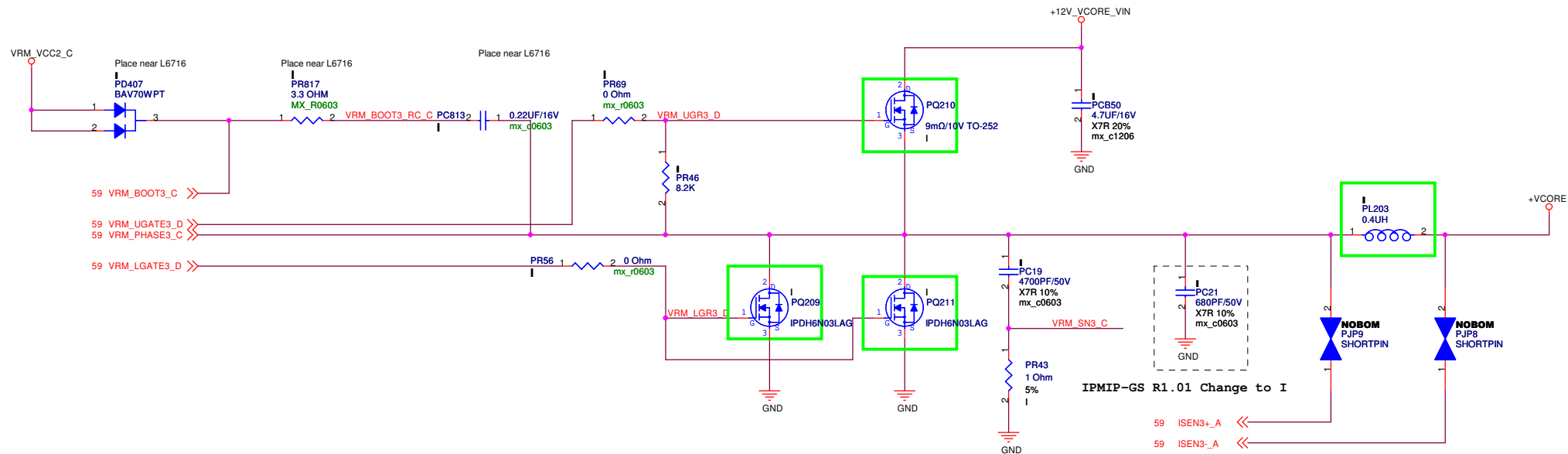
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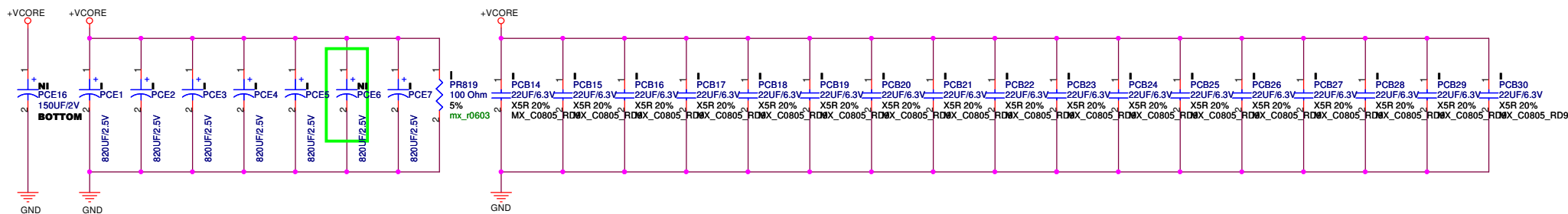
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+CPU Vcore OUTPUT CAPs

PEGATRON DT-MB RESTRICTED SECRET

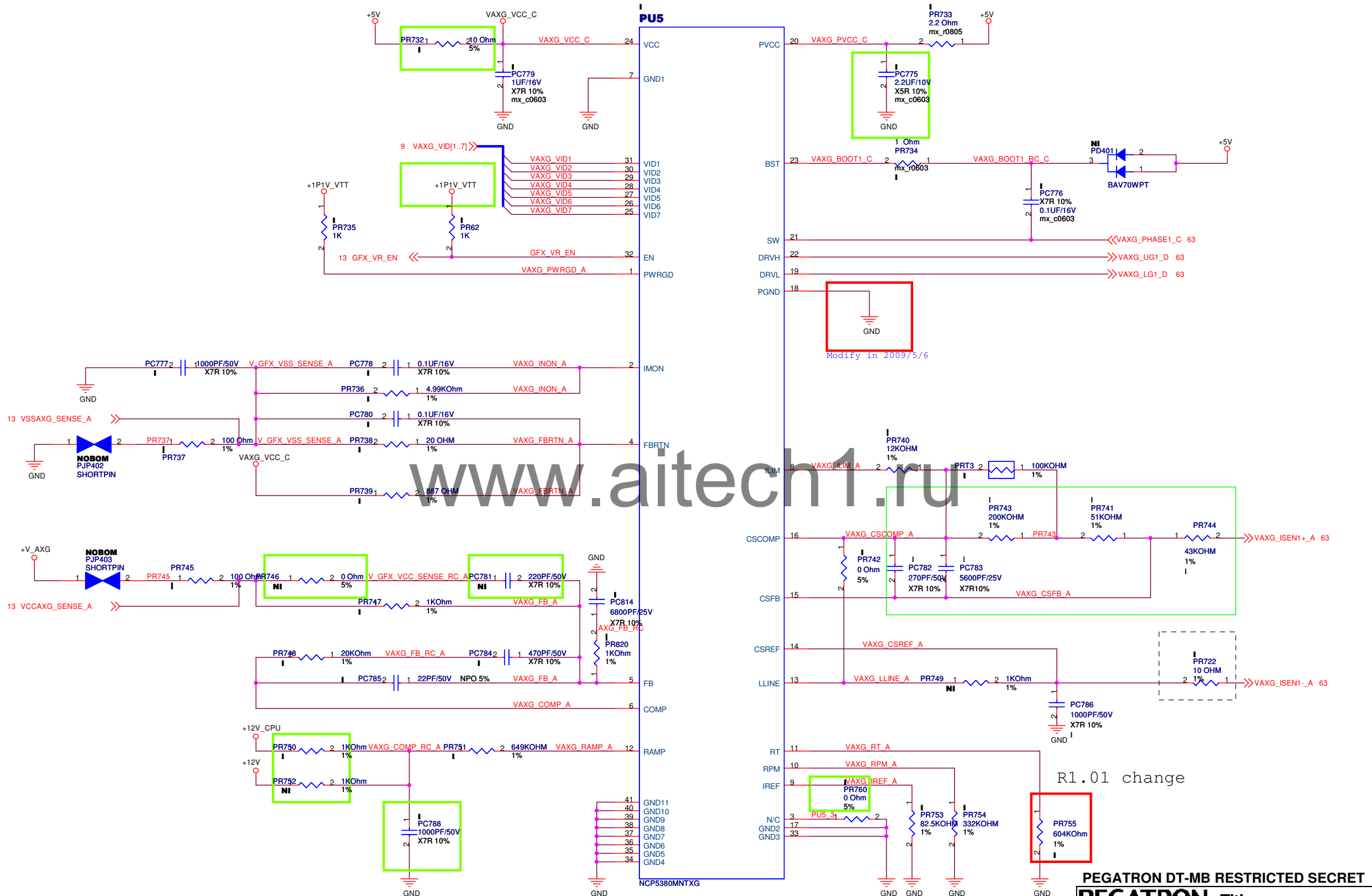
**PEGATRON** Title : Vcore DRIVER-2

Pegatron Corp. Engineer: Michael Lee

Size A3 Project Name IPMIP-DP

Date: Wednesday, April 07, 2010 Sheet 61 of 68

Rev 1.01



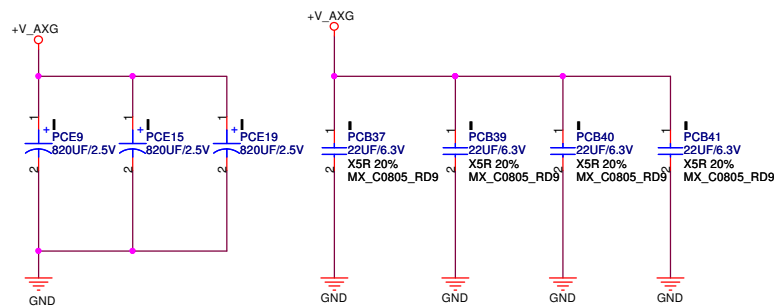
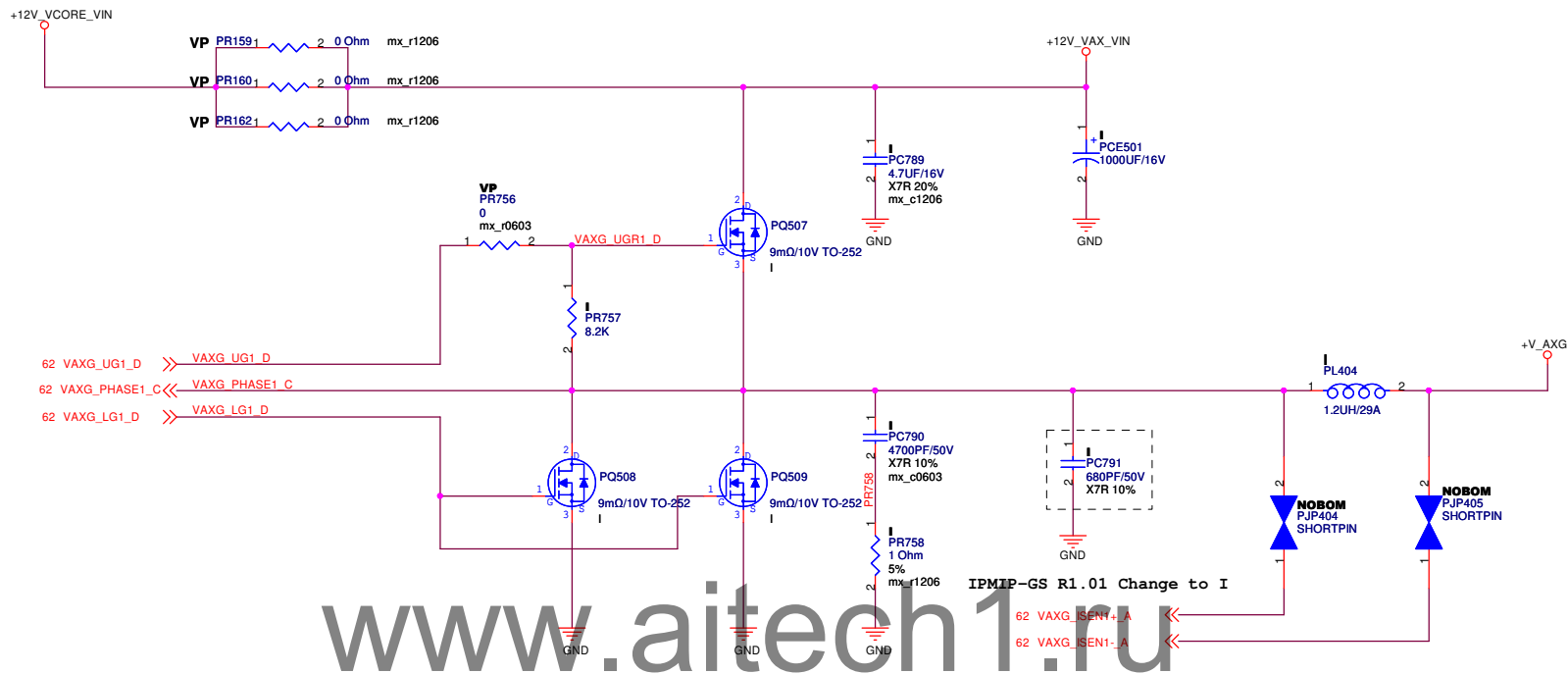
PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : VAGX CONTROLLER

Pegatron Corp. Engineer: Michael Lee

Size	Project Name	Rev
A3	IPMIP-DP	1.01

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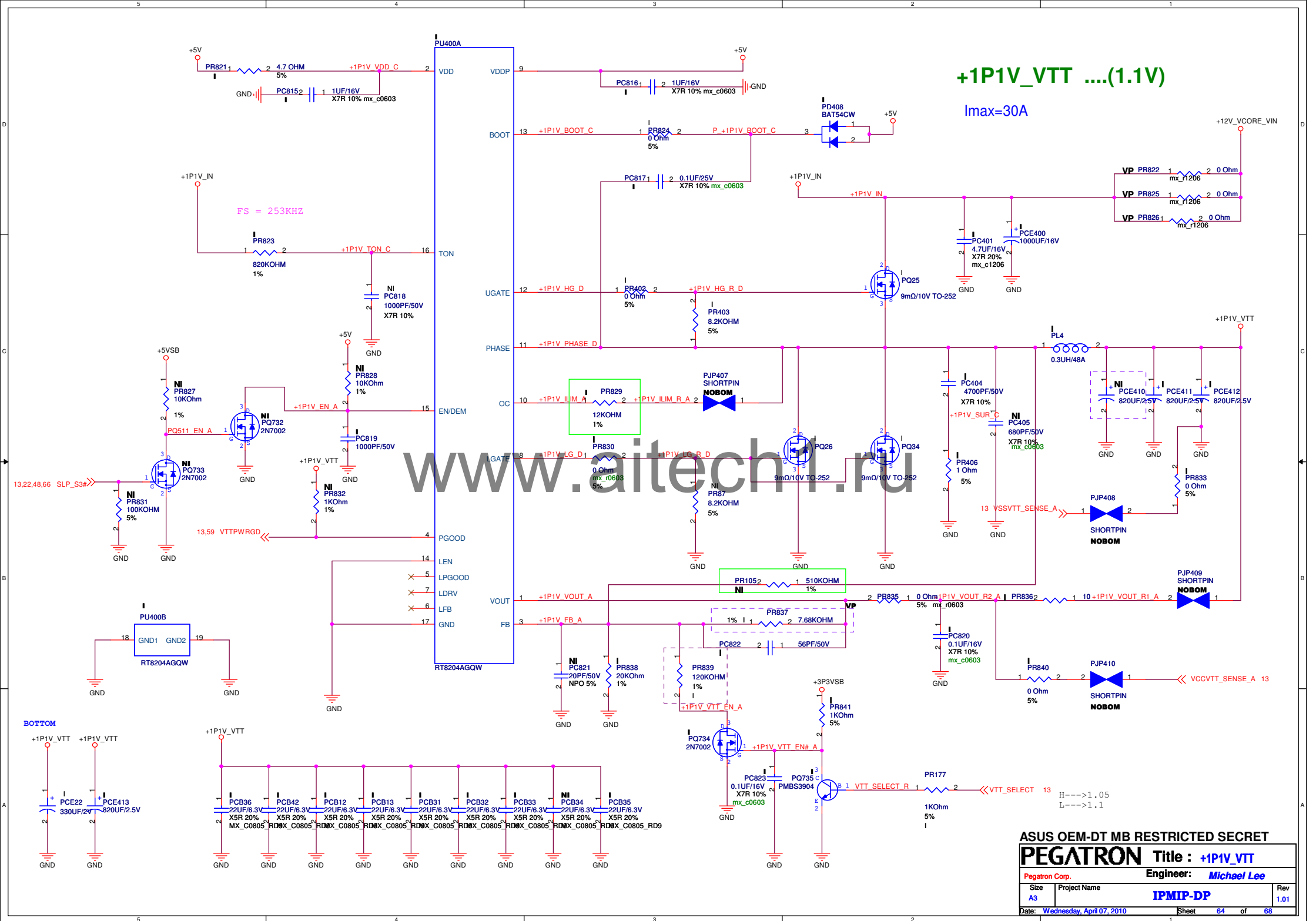


PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title : **VAGX DRIVER**

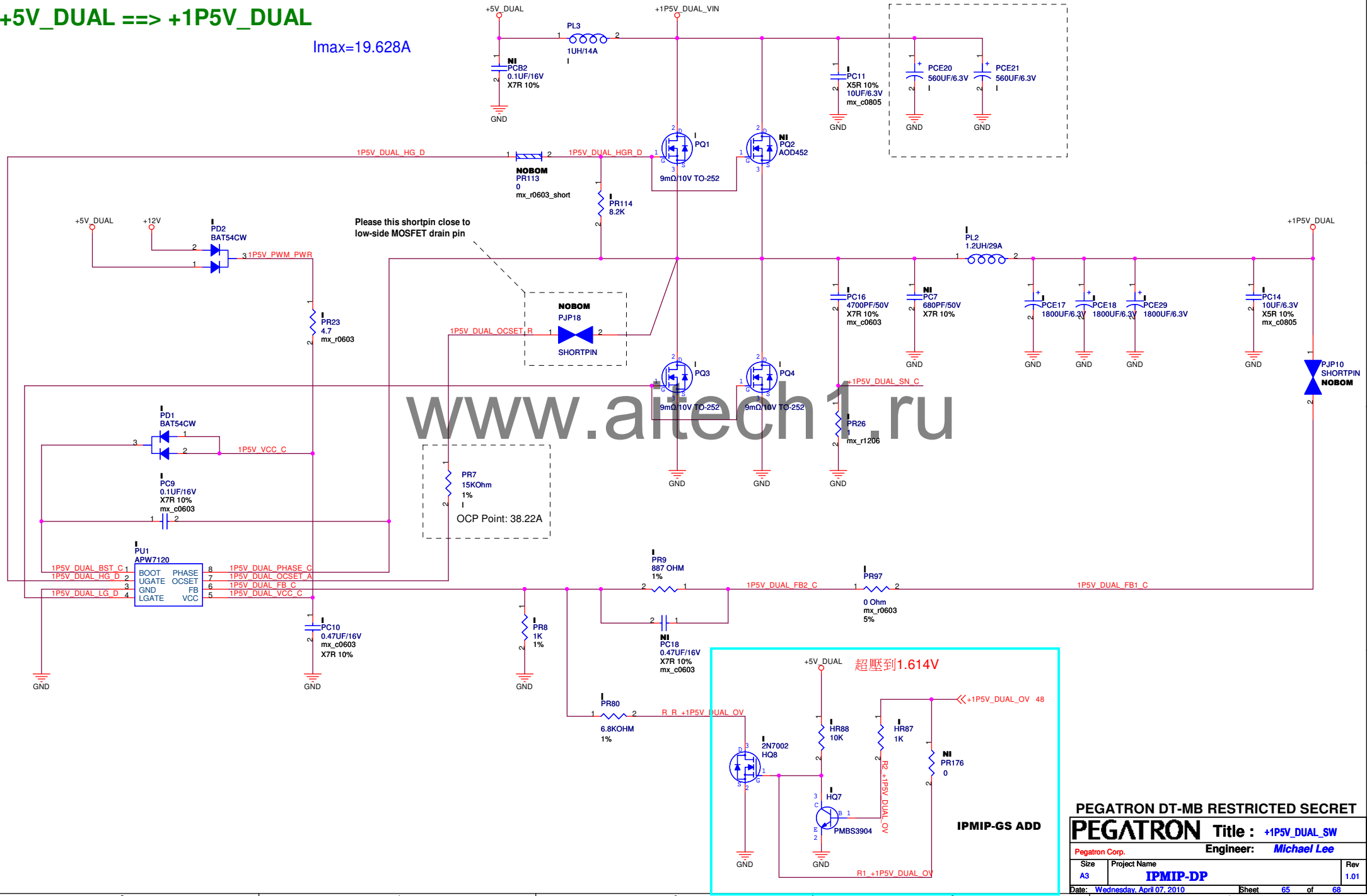
Pegatron Corp. Engineer: **Michael Lee**

Size A3	Project Name <b>IPMIP-DP</b>	Rev 1.01
Date: Wednesday, April 07, 2010	Sheet 63 of 68	



**+5V\_DUAL ==> +1P5V\_DUAL**

$I_{max}=19.628A$



PEGATRON DT-MB RESTRICTED SECRET

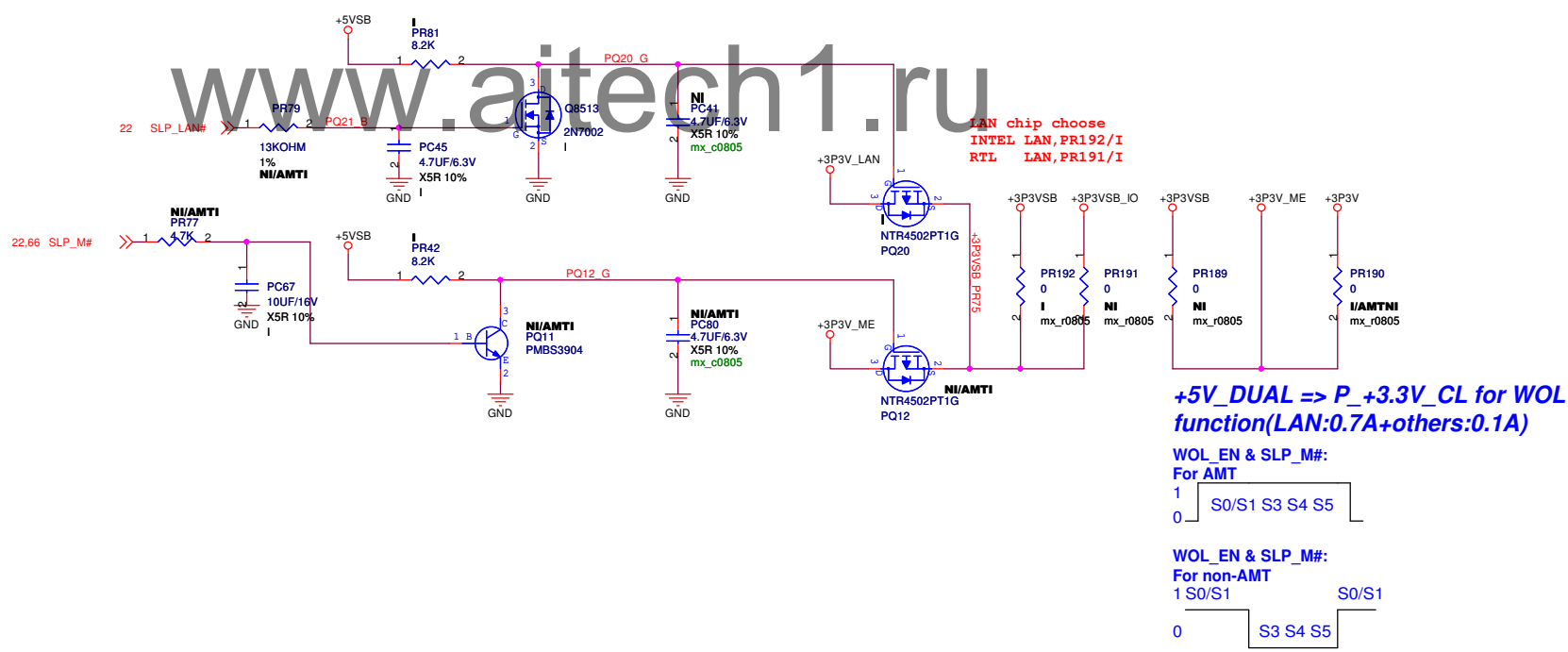
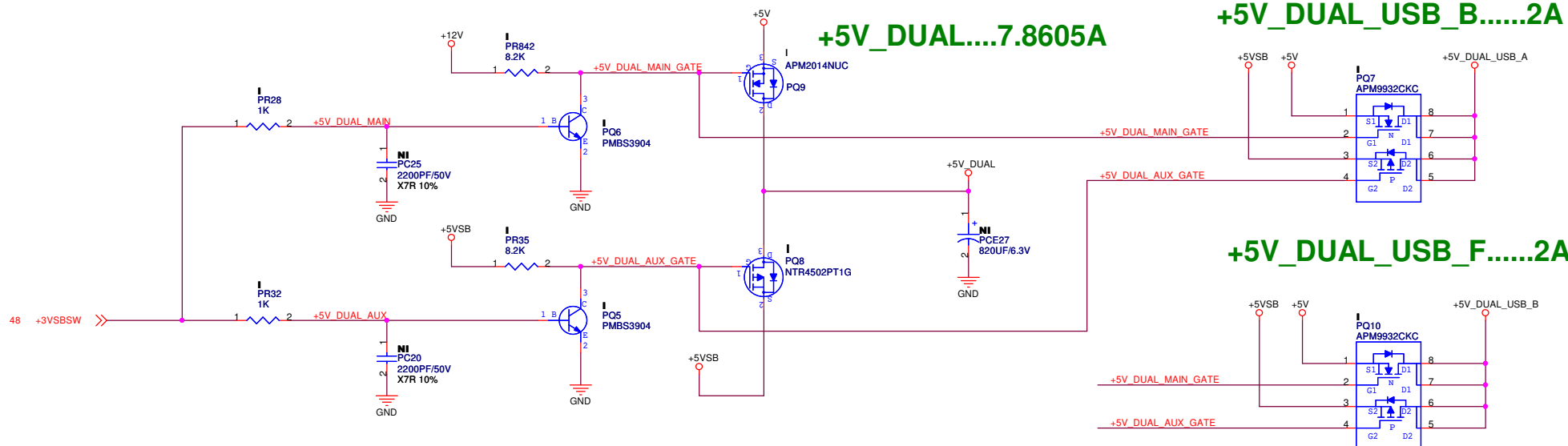
**PEGATRON** Title : **+1P5V\_DUAL\_SW**

Pegatron Corp. Engineer: **Michael Lee**

Size	Project Name	Rev
A3	<b>IPMIP-DP</b>	1.01

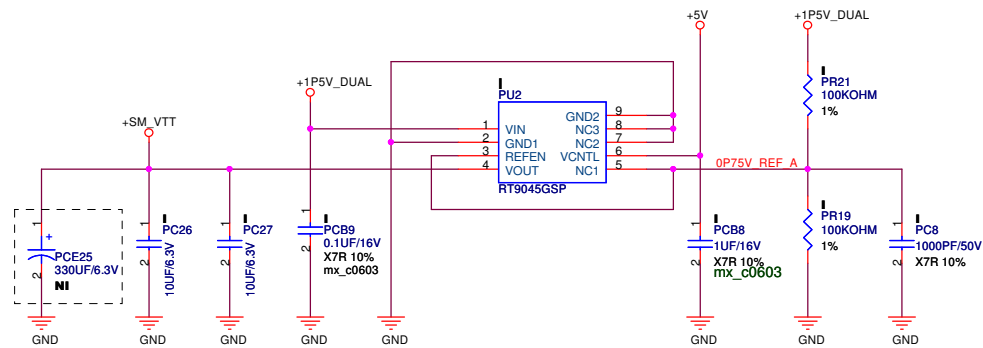
Date: Wednesday, April 07, 2010 Sheet 65 of 68





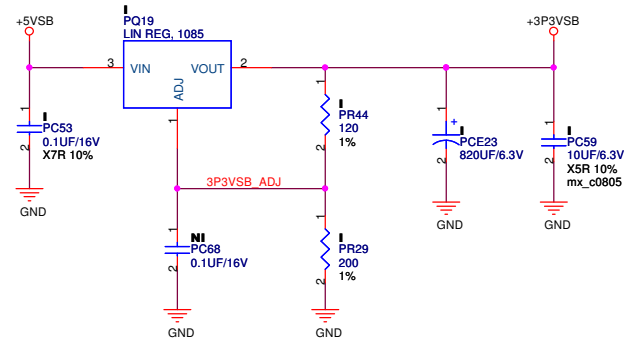
**+1P5V\_DUAL ==> +0P75V\_VTT\_DDR**

$I_{max}=0.83A$



4/28 MODIFY

**+5VSB ==> +3P3VSB....3.44A**



PEGATRON DT-MB RESTRICTED SECRET

**PEGATRON** Title: **+0P75V\_VTT\_ & +1P8V\_SFR**

Pegatron Corp. Engineer: **Michael Lee**

Size A3	Project Name <b>IPMIP-DP</b>	Rev 1.01
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